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(54) MEMORY CARTRIDGE AND MEMORY CONTROL METHOD

SPEICHERKASSETTE UND SPEICHERSTEUERVERFAHREN

CARTOUCHE MEMOIRE ET PROCEDE DE COMMANDE DE MEMOIRE

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EP 0 425 693 B1

Description

TECHNICAL FIELD

The present invention generally relates to memory cartridges and, more particularly, to a memory cartridge which has a dynamic random access memory DRAM incorporating a refresh circuit as indicated in the preamble of claim 1 and as eg. known from EP-A-0 128 427.

BACKGROUND ART

There have been widely used memory cartridges of a type in which an SRAM is back up by means of battery. As great reduction in the consumption power of a DRAM is recently realized, however, there has also appeared in the market memory cartridges of another type wherein the DRAM is back up by means of battery.

This is because the use of the DRAM can realize a memory capacity about 4 times larger than the use of the SRAM for the same size of memory. Accordingly, the use of the DRAM like the SRAM contributes greatly to increase in the memory capacity of the memory cartridge.

However, since the DRAM generally requires a refreshing time of several ten μ sec with a period of several msec, it is necessary to provide such a control circuit as to controllably adjust external access and refreshing operation. In addition, the memory cartridge of the SRAM type uses such a control signal as a chip enable signal having a format different from that used in the memory cartridge of the DRAM type and the SRAM type of memory cartridge is different in interface from the DRAM type of memory cartridge, which disadvantageously results in no compatibility between these SRAM and DRAM types.

A known example of battery for backing up the operation of such a memory cartridge is taught in a magazine titled "NIKKEI ELECTRONICS", August 10, 1987 (No. 427), pp. 167-183.

Conventional semiconductor memories capable of backing up information by means of battery include a flip-flop type static memory comprising 6 or 4 MOS transistors and two high resistances and a dynamic memory comprising a single MOS transistor and a single information storage capacitance (of several ten fF). The static memory, in particular, is suitable as a battery backup device because it requires a stationary (DC) consumption current as small as several ten nA or μA in a wait operation mode for the purpose of holding data. The dynamic memory, on the other hand, is suitably used in such a large-capacity memory system as called a semiconductor file which can have memory capacity 4 times larger than the static memory and can be more inexpensively made in cost per bit than the static memory when the same level of processing technique is employed. When the dynamic memory is back up by means of battery, however, this involves problems which follow. For this reason, the dynamic memory has not sufficiently been used as a portable semiconductor file memory.

Generally speaking, in the case of the dynamic memory, even when the memory shifts from its normal operation (active condition) mode wherein accessing is allowed for reading and writing operation to its wait operation (inactive condition) mode for the purpose of holding data, the memory must refresh (rewrite) data therein in a predetermined time. For example, in the case of a 1M bit memory, its refreshing period is set at usually 8 msec due to the limitation of the data holding time of the memory cells so that all the memory cells can be refreshed through 512 refreshing operations.

First one of problems in the above data holding operation, i.e., in the wait operation, is that the average consumption current of the dynamic memory necessary for the wait operation is as large as several hundred μA or mA. A second problem is that the peak level of a momentary AC current flowing in the refreshing-operation activation mode is as high as 100 mA or more.

As a measure against the former problem, it is most effective to prolong the refreshing period in the wait mode, as discussed in the aforementioned known literature.

The peak current as the latter problem is mainly due to the charging and discharging operation of the capacitances of bit lines connected to the memory cells. The total bit line capacitance for one refreshing operation amounts to several hundred pF and thus a momentarily large current flows through the memory. A memory system using the prior art dynamic memories causing such a peak current will be explained by referring to Figs. 1A and 1B.

More specifically, Fig. 1A is an arrangement of a battery backup type memory system 102, and Fig. 1B shows waveforms of peak currents flowing through power supply lines for the respective memories and of a peak current flowing through a common power supply line corresponding to a sum of the respective memory peak currents.

In Fig. 1A, the memory system 102 is made in the form of an easily portable file, a reader/writer 104 performs reading and writing operation from and to the memory system 102, a main power source 110 is a power supply means for the memory circuit 102, and a switch (SW) 114 is used to turn on or off the main power source 110. The memory system 102 includes a power supply circuit 108 for the memory system. The power supply circuit 108 in turn has an auxiliary power supply 112 for data backup as a second power supply means, diodes D_1 and D_2 for preventing a reverse current caused by a voltage drop in either one of the main and auxiliary power supplies 110 and 112 in the backup operation. The memory system 102 also includes memory chips M_1 to M_3, and capacitances C_1 for removal of high frequency noise components in the power supply. In Fig. 1B, reference symbols i_1 to i_3 denote the waveforms of the peak currents for the respective memory chips with

abscissa axis representing time t, and i_t denotes a sum of the peak currents i_1 to i_3 (= $i_1 + i_2 + i_3$) flowing through a common power supply line V_{cc}. In the drawing, the illustrated peak currents i_1 and i_3 have respectively two peaks overlapped together. This results from the fact that the dynamic memory of the present embodiment performs its self refreshing operation and varies in its oscillation period. Reference symbols r_1 and r_2 are respectively internal resistances for the main and auxiliary power supplies 110 and 112. The auxiliary power supply 112 is usually a dry cell and its internal resistance r_2 is as high as several Ω. The internal resistance r_1 of the main power supply 110 is smaller by one figure than the internal resistance r_2.

With such an arrangement, when the switch (SW) 114 is in its ON state, a current is supplied to the respective memory chips from the main power source 110 having the very low internal resistance r_1 so that, even when the peak current is large, the memory system 102 can normally execute its refreshing operation. When the SW 114 is in its OFF state, i.e., when the main power source 110 is in its cut-off state, on the other hand, a current is supplied from the auxiliary power supply 112, but since the auxiliary power source 112 has the internal resistance r_2 as high as several Ω, the momentary discharging current ability is low. As a result, the power supply voltage V_{cc} of the memory chips is remarkably reduced and the substrate potential is remarkably varied, which leads to the erroneous operation of the system.

As has been explained above, since the dynamic memory is large in its peak current, when such a small size battery as a button shaped battery having a large internal resistance is used, the momentary current supply ability becomes low. For this reason, even in the case of a small-capacity memory system, it becomes difficult to back up data for a long period of time or temporarily. Further, even when such a large-capacity cell as a lead battery is employed, it is difficult to realize the backup operation of such a large-capacity memory system that a multiplicity of dynamic memories are to be simultaneously refreshed, because the peak currents of the respective memory chips may be sufficiently considered to be overlapped together.

Fig. 2 shows an arrangement of a prior art dynamic memory system and a waveform of a peak current flowing through a power supply in its refreshing operation.

More in detail, an LSI chip 210 of Fig. 2A includes a memory array 212, an X-direction address buffer 214, a Y-direction address buffer 216, a data input/output (I/O) buffer 218, an X-direction decoder (XD) 220, a Y-direction decoder (YD) 222, and a data input/output signal line 224. The LSI chip 210 further includes a refreshing controller 226 having therein a self-refreshing timer, an address counter and elements associated with the refreshing operation. The memory array 212 includes dynamic memory cells MC, n word lines W for selection of the memory cells arranged in an X direction, and m bit lines B of the memory cells arranged in a Y direction. In Figs. 2A, reference symbol AX_i denotes a group of address signals for determining X-direction positions of the memory cells within the LSI chip 210, AY_i a group of address signals for determining Y-direction positions of the memory cells, I/O_i input/ output data signals, $\overline{REF}$ a refreshing control signal. This $\overline{REF}$ signal is considered to be externally input directly from outside of the chip or to be internally generated. Further, symbol V_{cc} is a power supply terminal in Fig. 2A, and a time T_c on the waveform of a peak current flowing through the power supply terminal V_{cc} in the refreshing operation represents a refreshing interval in Fig. 2B.

Generally speaking, in the case of a dynamic memory, it is necessary to refresh (rewrite) data within a predetermined time even when the memory system shifts from its normal operation (active condition) mode wherein accessing for reading and writing operations can be allowed to its wait operation (inactive condition) mode for holding the data. In the case of the aforementioned dynamic memory, when the refreshing control signal $\overline{REF}$ is activated, the memory system shifts from the normal mode to the wait mode, whereby a refreshing timer and an address counter incorporated in the chip are excited to automatically activate all the word lines sequentially and thereby refresh the data of all the memory cells. For example, in the case of a 1M bit memory, its refreshing period is set to be usually 8 msec due to the restriction of the data holding time of the memory cells so that all the memory cells can be refreshed through 512 refreshing operations. In this case, it is necessary to set one refreshing interval to be 8 msec per 512 and to select 2048 cells at one time at intervals of about 15 μsec, and the memory is set to have 2048 (=m) bits in the X direction and 512 (=n) bits in the Y direction.

In the dynamic memory, for such data holding operation as mentioned above, all the memory cells have been refreshed within a predetermined time (for example, within 8 msec in the above example) due to the restriction of the data holding time of the memory cells, even not only in the wait mode but also in the activated memory mode or normal mode (write/read accessing mode).

This has resulted in that the substrate potential is remarkably varied and/or the power supply voltage is remarkably reduced due to the internal resistance of a power supply cell when the memory is back up by means of the battery, which leads to the erroneous operation of the system. To overcome such disadvantages, it has been considered to make small device constants to thereby reduce the power consumption of the internal circuit, or to operate the memory at a low speed to realize small charging/discharging currents and thereby reduction in the level of the peak current. The latter measure of reducing the peak current in the refreshing operation, however, has found difficulties in also attaining the high access time of the memory and thus it has been difficult to actually carry out the current reducing measure.

EP-A-0 237 785 discloses a semiconductor memory apparatus wherein access signals and refresh signals are sequenced, wherein a precharge operation is performed between each access signal and refresh signal, and wherein the signal which happens to occur during the period of the other signal is stored and performed only when said other signal has been completed.

DISCLOSURE OF INVENTION

It is an object of the present invention to provide a memory cartridge which has a DRAM and is compatible with an SRAM memory cartridge.

Another object of the present invention is to provide a memory cartridge which has a circuit for adjusting accessing operation to a semiconductor memory device at high timing accuracy and which can realize a stable refreshing operation.

Yet another object of the present invention is to provide a semiconductor memory system which has an access time as high as a prior art in its normal operation mode and which is very small in the level of a peak current in a wait mode, i.e., in which data are merely held or backed up by means of power supply battery or the like.

Yet a further object of the present invention is to provide a semiconductor memory control system which can solve the above problems in the prior art, can realise its refreshing operation in a read accessing mode and can reliably hold data in a PSRAM.

According to the present invention there is provided a semiconductor memory apparatus as indicated in claim 1.

In embodiments of the present invention, the DRAM has a self refreshing circuit and a battery therein and is operated so that, when the DRAM is supplied with power from the external device, the DRAM performs its refreshing operation on the basis of an external refreshing signal received from the external device, while, when externally supplied with no power, it performs its self refreshing operation. The present invention may further comprise an access control circuit which detects a change in an address signal supplied from the external device and inverts for a predetermine period of time the logic level of the access signal for SRAM access such as a chip select signal, a chip enable signal, etc. supplied from the external device, whereby the DRAM is externally accessed as the SRAM.

There is further provided an access conversion circuit that converts an external SRAM access signal into a DRAM access signal. In this manner, the memory cartridge using the DRAM can be used in the same manner as in the memory cartridge using the SRAM and therefore a DRAM memory cartridge having a compatibility with an SRAM memory cartridge having a large memory capacity.

To this end, the access control means in the semiconductor memory system of the present invention is arranged so that at least two digit bits in a count value of a counter are allocated to four of a duration allowing generation of an access enable signal, a precharge duration for the access enable signal, a duration for generation of a refreshing enable signal, and a precharge duration for the refreshing enable signal, and the access arbitration circuit comprises a counter for counting a clock signal and means for generating the refreshing enable signal and receiving such memory access signals as a chip select signal and a chip enable signal when values of the two digit bits are allocated to the duration of generating the refreshing enable signal and for generating the access enable signal when the values of the two digit bits are allocated to the duration of generating the access enable signal.

In this way, since the four durations, i.e., the duration enabling the generation of the access enable signal, its precharge duration, the duration of generating the refreshing enable signal and its precharge duration can be allocated and managed depending on the value of the counter, these allocation timings can be accurately set at the same accuracy as the frequency of the counted clock signal, thus realizing the accurate access arbitration.

Thus, external signal timing can be set with high flexibility. In addition, when the frequency of the clock signal is increased, the probability of the DRAM being subjected to its refreshing operation can be made high. As a result, even when the DRAM is subjected to a long time access, there can be realized such a DRAM semiconductor memory system that can perform the SRAM function. In the case where a memory cartridge uses such SRAM, the memory cartridge can be advantageously made large in its memory capacity.

A resistance R and a capacitance C are connected respectively in series and in parallel to the power supply terminal of each of a plurality of memory chips. A second capacitance C_2 is provided in a common power supply line of the memory chips for supply of electric charges therethrough to the first capacitance C in the refreshing operation, for the purpose of preventing any drop in the power supply voltage even in the transient state of the power switching circuit when switched.

The waveform of the peak current flowing through each of the memory chip is smoothed through each smoothing circuit having a time constant τ = CR to reduce the peak level of the peak current. In addition, the value of the capacitance C is set so as to be positively recharged in the refreshing duration of each memory chip. The time constant τ is also determined taking into consideration the removal of noise in the power supply, external influences, and so on. This results in that a drop in the power supply voltage of each memory chip can be avoided and the optimum setting of the resistance R enables the power supply voltage drop in the normal and refreshing operations to be set at such an negligible level. As a result of having inserted the resistance R in a line connected to the power supply terminal of each

memory chip, a slight operational margin shortage such as an access time delay takes place but it is very minute or small when viewed from the entire memory system. The erroneous operation of the memory system due to the peak currents, on the other hand, is a very important problem but this problem can be eliminated by properly designing the system to have a sufficient operational margin.

An operational mode detecting means for detecting the operational mode enables the number of cells selected on word lines in a wait operational mode to be smaller than that in a normal operational mode in a memory cell array divided by an X-direction decoder.

The reduction of the value of the peak current is effectively attained by decreasing the number of selected cells in the refreshing operation, that is, by decreasing the number of bit lines chargeable or dischargeable at a time, which corresponds to increasing the number of refreshing operations to shorten its refreshing interval when the refreshing period is considered to be constant.

However, since the refreshing operation for activation of the memory and the write access operation belong to the same operational mode in the normal operation, the number of refreshing operations is increased as the refreshing interval is made shorter, whereby the access time is delayed undesirably to the system. Meanwhile, the wait operational mode for holding data based on the battery is an inactive condition to the memory, so that, even when the refreshing interval is shortened, this has no effect on the system and thus the refreshing interval in the wait mode can be set shorter than that in the activation mode.

For the above reason, in the normal operation mode, a predetermined number of cells connected to word lines corresponding to the outputs of the X-direction decoder XD are refreshed providing no influence to the access time of the memory. In the wait operational mode, on the other hand, a mode switching signal of the operational mode detecting means causes the activation of the internal circuit, whereby the number of memory cells connected to word lines corresponding to the outputs of the X-direction decoder XD is reduced, the capacity of the bit lines is minimized, and the charging/discharging current, i.e., the peak current in the refreshing operation is decreased.

For the purpose of attaining the above object, in accordance with the present invention, a read access enable signal generated in the read access mode is set to have a constant time width, a data is read out from the memory at the end of the read access operation based on the read access enable signal, and the read data is latched in a latch circuit.

It is during the duration of the read access enable signal that the PSRAM is actually in the read access mode. When the duration of the read access enable signal is terminated, the PSRAM is released from the read access mode, but the read data is latched from the release time point and thus the refreshing operation can be carried out.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1A is an arrangement of a prior art memory system;

Fig. 1B shows waveforms of peak currents flowing through memory chips in a refreshing operation;

Fig. 2A is a block diagram of a prior art semiconductor memory system;

Fig. 2B shows wave forms of a peak current in normal and wait operation modes;

Fig. 3 shows a circuit configuration of a memory card using a PSRAM in accordance with the present invention;

Fig. 4 is a block diagram showing a specific example of an access control circuit;

Figs. 5A and 5B are timing charts for explaining the access operation;

Fig. 6 is a block diagram showing an access mediating circuit in the access control circuit;

Fig. 7 is a diagram for explaining how to allocate access periods;

Fig. 8 is a block diagram showing an exemplary internal arrangement of a virtual SRAM;

Fig. 9 is a block diagram of the access mediating circuit in the semiconductor system;

Fig. 10A is a circuit arrangement for explaining the principle of a memory system in accordance with an embodiment of the present invention;

Fig. 10B shows waveforms of peak currents flowing through memory chips in a refreshing operation;

Figs. 11A and 11B are a block diagram and a timing chart for explaining how to specifically control the memory system based on a refreshing control signal;

Fig. 12 is a specific application example of the memory system of the present invention;

Fig. 13 shows a particular array of electronic parts used in the present invention;

Fig. 14A is a block diagram for explaining the principle of a semiconductor system in accordance with

another embodiment of the present invention;

Fig. 14B shows a wave form of a peak current, together with a waveform of a mode switching signal, in normal and wait operation modes;

Figs. 15A and 15B show a detailed example of an operational mode detecting means in Fig. 14A and a timing chart for explaining the operation thereof, respectively;

Fig. 16 is a block diagram of a detailed semiconductor memory system in accordance with a further embodiment of the present invention;

Fig. 17 is a timing chart for explaining the operation of an access mediating part in the system of Fig. 16;

Fig. 18 is a timing chart for explaining the operation of a chip enable signal converting part in the system of Fig. 16;

Fig. 19 is a block diagram showing an embodiment of a semiconductor memory control system in accordance with the present invention;

Fig. 20 is a timing chart for explaining the operation of the embodiment of Fig. 19;

Fig. 21 is a block diagram showing another embodiment of the semiconductor memory control system in accordance with the present invention; and

Figs. 22A to 22C show timing charts for explaining the operation of the embodiment of Fig. 21.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring first to Fig. 3, there is shown a block diagram of an embodiment wherein a semiconductor system of the present invention is applied to a memory cartridge 301. More specifically, the memory cartridge 301, which is connected to such a data processing apparatus as a computer through a connector 310, includes a pseudo SRAM array (which will sometimes be referred to as the PSRAM, hereinafter) 320 which in turn incorporates a self refreshing circuit 320a.

Also included in the memory cartridge 301 to send control signals from the external data processing apparatus to the PSRAM 320 is an access control circuit 319 which is provided between control terminals of the connector 310 for chip enable ($\overline{CE}$) output enable ($\overline{OE}$) and write enable ($\overline{WE}$) signals and control terminals of the PSRAM 320 (including address terminals $\overline{CE}$, $\overline{OE}$ and $\overline{WE}$ and a refresh terminal $\overline{RFSH}$). Further included in the memory cartridge 301 is a clock generating circuit 318 which supplies a clock signal to the PSRAM 320 and other circuits therein.

The self refreshing circuit incorporated in the PSRAM 320 functions to automatically perform its self refreshing operation based on the electric power of a backup cell to hold data therein in a wait mode in which the memory cartridge is supplied with no power from an external device. Thus, the memory cartridge can eliminate the need for performing any refreshing operation based on the external device. In a normal operation mode in which the memory cartridge is supplied with external power, however, the external refreshing operation is required and the refreshing request signal is generated, in the illustrated embodiment, at the access controller 319.

A power switching circuit 312, which has a diode and so on, is provided to switch between the external power supply and internal power supply battery. More in detail, the power switching circuit 312 is inserted between a power supply line 310a connected to a power supply terminal of the connector 10 and a power supply terminal V_{cc} of the PSRAM 320 so that, when the memory cartridge 301 is connected to the external data processor, the PSRAM 320 can receive power from the external data processor. That is, the power switching circuit 312 acts to supply power from the power supply terminal of the connector 310 to the power supply terminal V_{cc} of the PSRAM 320 and also when the circuit 312 is not supplied with this power, to supply power from a power supply battery 311 to the power supply terminal V_{cc} of the PSRAM 320.

Connected to the power supply line 310a connected to a power supply terminal of the connector 310 is a voltage detector 313 which detects a voltage on the line 310a and sends the detected voltage output to a mode switching circuit 317. The circuit 317 in turn judges, on the votlage output received from the voltage detector 313, whether or not the memory cartridge 301 is connected to the external data processor and sends a corresponding mode signal to the access controller 319.

An address buffer 315 is inserted between an address signal line 310b connected to the connector 310 and an address terminal Addr of the PSRAM 320 so that the PSRAM 320 can receive an address signal from the external data processor. Also connected to the address signal line 310b of the connector 310 are a decoder 314 and the access controller 319, so that the access controller 319, when receiving a decoded-address output from the decoder 314, can be started.

A data buffer 316 for input/output of data is provided between a data signal line 310d connected to the connector 310 and the data terminal I/O of the PSRAM 320 to perform data transfer between the external data processor and the PSRAM 320.

The access controller 319 has, as shown in Fig. 4, an access arbitration circuit 419a, a chip enable signal conversion circuit 419b and a refreshing timer 419c to receive the address signal and the control signals of the chip enable signal ($\overline{CE}$, output enable signal $\overline{OE}$ and write enable $\overline{WE}$ signals from a control signal line 310c

of the connector 310.

The access arbitration circuit 419a may be an R-S flip-flop which comprises, for example, NAND circuits 406a and 406b having delay circuits 405a and 405b inserted in their output feedback circuits, an output of the NAND circuit 406a being used as an access enable signal $\overline{ACCESS}$ to the PSRAM 320, an output of the NAND circuit 406b being used as a refreshing enable signal $\overline{REFRESH}$ to the PSRAM 320. And either one of the chip enable signal $\overline{CE}$ supplied from the external device and the refreshing request signal $\overline{REFH}$ supplied from the refreshing timer 419c which is supplied first disables the other signal.

The access enable signal is applied to a gate signal 404 in the chip enable signal conversion circuit 419b as its gate signal to be converted into a chip enable signal $\overline{CE_p}$

The chip enable signal conversion circuit 419b having such an arrangement as illustrated functions to convert the chip enable signal $\overline{CE}$ from the connector 310 at the timing of the SRAM into the chip enable signal which conforms in format to the pseudo SRAM.

Meanwhile, in the SRAM, when the chip enable signal $\overline{CE}$ (or chip select signal $\overline{CS}$ included in the chip enable signal which will be explained later) is fixed to a low level (L), reading of a data from a predetermined address can be attained by varying the address signal. In the pseudo SRAM, however, since reading operation is carried out at a clocked interface, it is necessary to clock the chip enable signal $\overline{CE}$. Fig. 5A shows waveforms of the signals $\overline{Addr}$, $\overline{CE}$ and $\overline{OE}$ when the SRAM is accessed for reading data. The signal $\overline{Addr}$ is a timing address signal and the chip enable signal $\overline{CE}$ is maintained at level "L" even when the address signal varies. The output enable signal $\overline{OE}$ is maintained also at level "L".

Explanation will next be made as to the reading operation of the chip enable signal conversion circuit 419b. Fig. 5B shows a timing chart when the pseudo SRAM is accessed. In the drawing, the signal $\overline{Addr}$ is a timing address signal and the chip enable signal $\overline{CE_p}$ is a clock signal having a predetermined clock width which, as the address signal varies, is maintained at high (H) level for a constant duration t_p necessary for the precharging of the memory and then changed to low level "L". The output enable signal $\overline{OE_p}$ is kept at level "L" even when the address signal varies and thus the accessing operation of the SRAM can be similarly applied to the pseudo SRAM. The address signal is received from the address signal line 310b.

Further, the write enable signal $\overline{WE_p}$ is maintained at level "H" in the reading operation even when the address signal varies. An output data signal I/O_p has an effective data duration in which an effective data is present and which appears a chip enable signal access time duration t_{co} later after the chip enable signal $\overline{CE_p}$ falls to level "L".

The chip enable signal conversion circuit 419b, as shown in Fig. 4, detects a change in the address signal and generates the chip enable signal $\overline{CE_p}$. In the circuit 419b, more in detail, EXOR circuits 2a, 2b, ..., and 2n perform exclusive "OR" operations over the digit bits of the address signal and their delay signals, respectively, and an OR circuit 403 performs an "OR" operation over output signals of the EXOR circuits 402a, 402b, ..., and 402n and the external chip enable signal $\overline{CE}$. That is, in response to a variation in the address signal, the EXOR circuits 402a, 402b, ..., and 402n are operated so that the OR circuit 403 produces the chip enable signal $\overline{CE_p}$ having a "H" level duration corresponding to the operated period of the EXOR circuits and having an "L" level duration. The chip enable signal $\overline{CE_p}$ thus obtained is applied from the OR circuit 403 through a gate circuit 404 to the chip enable terminal $\overline{CE}$ of the PSRAM 320. The "H" duration of the chip enable signal CE_p can be adjusted by inserting a suitable delay circuit and further taking a logical sum, and the rising timing of the chip enable signal $\overline{CE_p}$ at which the signal becomes significant can be adjusted.

Now, when the memory cartridge 301 is mounted in the data processor through the connector 310, the access control circuit 319 receives a connection mode signal from the mode select circuit 317. At this time, if the mode signal is indicative of the memory cartridge 301 connected to the external data processor and the address signal to be accessed by the external data processor selects the memory cartridge 301, then the address signal is decoded at the decoder 314 and applied to the chip enable signal conversion circuit 419b of the access controller 319. The circuit 419b, when receiving the chip enable signal $\overline{CE}$ from the data processor together with the decoded address signal, generates the chip enable signal $\overline{CE_p}$ at such timing as shown in Fig. 5B.

As already explained above, when the chip enable signal conversion circuit 419b receives the chip enable signal $\overline{CE}$, the circuit 419b detects a variation in the address signal Addr and converts the chip enable signal CE into such a chip enable signal $\overline{CE_p}$ having a level "H" for a constant duration after the timing of the address signal variation and then having a level "L" thereafter as shown in Fig. 5B. The converted chip enable signal CE_p can be sent to the terminal CE of the PSRAM 320 during generation of the aforementioned access enable signal of the access adjusting circuit 419a.

As a result, the data buffer 316 receives an enable signal from the access controller 319 after the chip enable signal access period t_{co} from the falling of the chip enable signal CE_p and stores therein an effective data received from the I/O terminal of the SRAM 320. At this time, a write enable signal ("H") externally entered is sent as it is sent to the terminal WE of the PSRAM 320 as the write enable signal $\overline{WE_p}$.

The writing operation to the memory cartridge 301 is carried out when the write enable signal WE changes from its level "H" to level "L" and explanation thereof is

omitted because it is substantially the same as in the case of the SRAM.

In this manner, the duration t_p of the chip enable signal necessary for the precharging of the memory is secured and then the chip enable signal is made at level "L" to convert access based on address clock into a CE clock at the access arbitration circuit, and after the constant period t_{co}, the effective data is stored in the data buffer 316.

Explanation will next be made as to another example of the access control circuit.

Fig. 6 shows another such detailed exemplary access arbitration circuit 630 that allows access arbitration not only to the PSRAM 320 incorporating a self refreshing circuit but also to the DRAM and that the refreshing enable signal and access enable signal can be controlled on the basis of a clock signal issued from an external device (or on the basis of a clock signal issued from a clock in the clock generator 318).

The access arbitration circuit 630 of Fig. 6 has a counter 621 and a data latch flip-flop (D-F/F) 622. The counter 621, when receiving a clock signal at a clock input terminal 626 sent from the external device (or the clock generating circuit 318 incorporated in the memory cartridge 301) which is connected with the memory cartridge 301, counts the clock signal and is operated according to the counted value.

More concretely, the counter 621 is an n-notation counter which receives at its clock terminal CK, for example, a clock signal having a period of about 50 nsec and secures a duration allowing the generation of an access enable signal, its precharging duration, a duration allowing the generation of a refreshing enable signal and its precharging duration. One output of the counter 621 at its output terminal Q_{n-1} is sent to respective first input terminals of a 2-input OR gate 623 and a 3-input OR gate 624, while the other output of the counter 621 at its output terminal Q_n is applied to a second input terminal of the OR gate 623 through an inverter 623a. The Q_n output of the counter 612 is also applied to a second input terminal of the OR gate 624 and to a first input terminal of an OR circuit 625 directly without intervention of any inverter.

The OR gate 623 is a negative logic circuit which receives the Q_n output from the counter 621 and the Q_{n-1} through the inverter 623a from the counter 621 to regard a negative logic output (having low level "L") as significant. More specifically, the OR gate 623, when the Q_{n-1} output of the counter 621 is at level "L" and the Q_n output thereof is at level "H", generates at its output terminal a negative logic refreshing enable signal $\overline{\text{REFRESH}}$ having level "L". In other words, so long as the values of the outputs Q_n and Q_{n-1} are "0" and "1" respectively, the counter 621 generates the refreshing enable signal.

The OR gate 624 is also a negative logic circuit which receives at its third input terminal the chip enable signal $\overline{\text{CE}}$ from an input terminal 627. Only when the values of the outputs Q_n and Q_{n-1} are both "0", the OR gate 624 generates a negative logic signal ACCESS of level "L". In other words, when the values of the outputs Q_n and Q_{n-1} are not both "0", either one of these outputs is at level "H", so that, even when the OR gate 624 receives the chip enable signal $\overline{\text{CE}}$, the gate 624 will not generate the negative logic access enable signal $\overline{\text{ACCESS}}$. That is, only when the values of the outputs Q_n and Q_{n-1} are both "0", the access enable signal is generated.

Meanwhile, the OR circuit 625 receives the output Q_n from the counter 621 and the access enable signal from the OR circuit 624 and sends its output to a terminal D of the D-F/F 622.

The D-F/F 622 receives at its clock terminal CK from the clock input terminal 626 through an inverter 622a and latches an output of the OR circuit 625. More specifically, the D-F/F 622, when the latch data becomes "0", an output of the D-F/F generated at its output terminal Q is shifted from level "H" to "L" and the D-F/F resets the counter 621 at a timing when the Q output is shifted from level "H" to "L" whereby the counter 621 is restarted from its count value "0". At this restart time, the values of the outputs Q_n and Q_{n-1} of the counter 621 are both "0", so that, when the chip enable signal $\overline{\text{CE}}$ is generated, the signal $\overline{\text{CE}}$ is passed through the OR gate 624 and the access enable signal is generated.

The above operational relationship between the access enable signal and refreshing signal is summarized as shown in Fig. 7.

When the counter 621 is an up counter and resetting thereof in the course thereof is not considered into consideration, the count values of the outputs Q_n and Q_{n-1} of the counter 621 are changed sequentially in the order of "0", "0"; "1", "0"; "0", "1"; "1", "1"; and "0", "0".

More concretely, a duration wherein the count values of the outputs Q_n and Q_{n-1} of the counter 621 are "0" and "0" respectively (duration of the count values from "0", "0" to "1", "0") is an access enable duration during which, when the chip select signal is changed to level "L", the access enable signal is generated. A duration wherein the count values of the outputs Q_n and Q_{n-1} of the counter 621 are "0" and "1" respectively is a refreshing enable duration, during which, even when the chip select signal is changed to level "L", no access enable signal is generated and only the refreshing enable signal is generated as effective. A duration wherein the count values of the outputs Q_n and Q_{n-1} of the counter 621 are "1" and "0" respectively is a precharging duration to the access enable signal, and a duration wherein the count values of the outputs Q_n and Q_{n-1} of the counter 621 are "1" and "1" respectively is a precharging duration to the refreshing enable signal.

It is considered that, when the access enable signal is generated immediately before the change of the values of the outputs Q_n and Q_{n-1} from "0", "0" to "1", "0", the precharging duration becomes insufficient. For the purpose of preventing it, the present invention is arranged so that, when the chip select signal is changed

to level "L", the D-F/F 622 resets the counter 621 to start the recounting of the counter 621. This is first one of the reasons why the D-F/F 622 and the OR circuit 625 are provided to reset the counter 621. Further, when the values of the outputs Q_n and Q_{n-1} are changed from "1", "1" to "0", "0", the counter 621 is reset to restart its counting operation from zero count. This is the second one of the reasons why the D-F/F 622 and the OR circuit 625 are provided to reset the counter 621 through the OR circuit 625. If the duration wherein the values of the outputs Q_n and Q_{n-1} are "1" and "0" is sufficient, then the precharging duration can be obtained, so that the need for such resetting based on the chip select signal as mentioned above can be eliminated. When the access enable duration is set sufficient and the counter 621 is a circulating counter, the count value of the counter 621 is again returned to "0", so that the resetting based on the Q_n output of the counter 621 can be eliminated.

In this manner, the generation of the access enable signal is prevented during a period from the change of the Q_{n-1} digit of the counter 621 to "1" to the resetting of the next Q_{n-1} and Q_n digits at "0" and "0". And the period for preventing the generation of the access enable signal can be allocated as the refreshing duration and precharging duration. Similarly, since the counter is reset at the time of generating the access enable signal, a duration from the counting start "0" to "0", "0" corresponds to the access enable duration and thus the generation of the access enable signal is prevented until the refreshing enable duration wherein the values are "0" and "1".

That is, by dividing the frequency of the externally supplied clock signal externally through the counter, the refreshing enable signal $\overline{\text{REFRESH}}$ and the access enable signal $\overline{\text{ACCESS}}$ can be generated independently of each other.

In the event where the frequency of the clock signal is set high, even when the chip enable signal last for a long period of time, the probability of generating the refreshing enable signal becomes high and the refreshing generation period can be set shorter than the prior art. Accordingly, one or more refreshing operations can be positively realized during the refreshing period of the prior art, so that, even when access is frequently carried out, refreshing can be obtained between the accessing operations, thus resulting in that it can be avoided that such period that refreshing cannot be effected lasts.

In this access arbitration circuit, the values of two digits of the counter are allocated to the access enable duration, the refreshing enable duration, and the precharging durations thereto, but the number of such digits of the counter is not limited to the particular 2 and may be 3 or more so long as the allocation of 4 or more durations is allowed.

The counter 621 comprises an up counter in the illustrated embodiment, but the type of the counter is not limited to the particular type and may be a down type or other suitable type.

Although the clock signal to be counted at the counter 621 has been externally obtained in the foregoing embodiment, the clock signal may be a clock signal used in the interior of a microprocessor, a clock signal generated at the machine cycle, or a clock signal as a control reference signal supplied from a clock generating circuit to the microprocessor.

Though the foregoing embodiment has been explained in connection with the case of the PSRAM, when a refreshing circuit is provided within the memory cartridge but outside the RAM, the cell refreshing circuit within the PSRAM can be made unnecessary and a DRAM can be used in place of the PSRAM. Accordingly, the present invention may comprise a memory cartridge having the DRAM and the refreshing circuit. In this case, the chip enable signal conversion circuit 419b in the embodiment is replaced by an access conversion circuit for converting an SRAM access signal into a DRAM access signal.

The memory cartridge in the present specification may be made in the form of a card or in any shape called a memory card or a cassette memory.

As will be appreciated from the foregoing explanation, in accordance with the present invention, since the access conversion circuit for converting an external SRAM access signal into a DRAM access signal is provided, the memory cartridge using the DRAM can be used in the same manner as the memory cartridge using the SRAM, whereby a memory cartridge compatible with that using the SRAM having a large memory capacity can be realized.

Shown in Fig. 8 is an internal arrangement of a semiconductor system in accordance with another embodiment, which includes a DRAM memory cell matrix 801, a row address latch circuit in an X decoder system, an X decoder 802b, a column address latch circuit 803a in a Y decoder system, a Y decoder 803b, a write circuit 803c and a sense amplifier 803d.

In operation, an external address signal is once stored in an address buffer 804 to be divided into component signals in row and column direction, which are then supplied to and stored in the row and column address latch circuits 802a and 803a respectively. These stored data are decoded at the respective X and Y decoders. In a write operation, the write circuit 803c is controlled by a timing controller 806, a data received from an I/O circuit 805 is decoded at the X and Y decoders 802b and 803b to be written at an intersection position of the matrix as a one bit data. The data reading operation is carried out in a manner opposite to the aforementioned data writing operation.

A refreshing address counter 807 sequentially scans the X decoder system by the number of the rows at refreshing timing in a refreshing cycle (refreshing duration) according to a signal received from the timing controller 806. In this manner, in the refreshing cycle, the cycle reading operation is carried out under the timing controller 806 so that the DRAM memory cell matrix

801 is refreshed. The refreshing timing is provided by receiving at the timing controller 806 a refreshing request signal RFSH cyclically generated at a refreshing timer 808.

The timing controller 806 receives from external circuits such signals as a chip enable signal $\overline{CE}$, an output enable signal $\overline{OE}$ and a write enable signal $\overline{WE}$. The timing controller 806 incorporates an access arbitration circuit 809 which controls access competition to the SRAM memory cell matrix 801 between the chip enable signal $\overline{CE}$ received from the external device and the refreshing request signal $\overline{RFSH}$ received from the refreshing timer 808.

An access arbitration circuit 900 shown in Fig. 9 is made in the form of an R-S flip-flop which comprises NAND circuits 909a and 909b having delay circuits ($\overline{DELAY}$) 910a and 910b inserted in their output feedback circuits. An output of the NAND circuit is used as the access enable signal $\overline{ACCESS}$ to the DRAM memory cell matrix 801 while an output of the NAND circuit 909b is used as the refreshing enable signal $\overline{REFRESH}$ to the DRAM memory cell matrix 801.

Fig. 10 shows another embodiment of the present invention, wherein Fig. 10A shows an arrangement of a memory system of the embodiment and Fig. 10B shows waveforms of peak currents in the refreshing operation of dynamic memory chips in the embodiment. In Fig. 10A, reference numeral 1002 denotes a memory system in the form of a portable file, 1004 a reader/writer for performing reading and writing operations from and to the memory system 1002, 1006 a memory section including memory chips M_1 to M_3 and smoothing circuits connected to respective power supply terminals of the memory chips, 1008 a power supply including an auxiliary power supply, a main power source and power switching circuit.

The peak currents flowing through respective memory chips in the refreshing operation have such waveforms as shown in Fig. 10B. More in detail, a peak current i_1 to the memory chip M_1 is supplied from electric charges charged in a capacitance C and the capacitance C is again charged in an inactive duration of the refreshing period. For this reason, a current i_1' as viewed from the side of a common power supply line V_{CC} is made smoother and lower in level than the current i_1. Similarly, peak currents i_2' and i_3' for the other memory chips M_2 and M_3 are also made lower. Therefore, a total peak current i_t' of such peak currents i_1', i_2' and i_3' is also made lower than the corresponding one in the prior art of Fig. 1, so that a power voltage drop due to the internal resistance of an auxiliary power supply 1012 can be made small.

The value of the capacitance C is set taking into consideration a time during which recharging can be sufficiently effected in the refreshing period, the amount of charge allowing the sufficient replenishment of the peak current, and the role of removing noise in the power supply. Accordingly, a time constant $\tau = C*R$ is set to be sufficiently short as compared with the refreshing period and also to allow the reduction of the peak current level in the refreshing operation. The value of a resistance R is determined to be in a range where the voltage drop can be sufficiently ignored in the write/read access active operation and in the refreshing operation. For example, when the oscillation period in the refreshing operation is 50 μsec., a charging time of 5 μsec. or less providing one-figure allowance is set, the value of the capacitance C is set to be between 0.1 and 0.5 μF, and the value of the resistance R is set to be about between 5 and 10 Ω, so that the voltage drop can be suppressed by about 0.2 V or less at the maximum level of the peak current of the memory chip and therefore the internal erroneous operation can be eliminated. Since the supply of electric charges to the first capacitance C in the refreshing operation is necessary even in a transient state of the power switching circuit caused by its switching operation, a second capacitance C_2 is set to have a value sufficiently larger than a product of the number of memory chips used and the value of the capacitance C.

In the foregoing embodiment, the peak currents are made smooth through the series-connected resistances R and parallel-connected capacitances C to the respective memory chips independently of each other, whereby the level reduction of the peak currents can be attained only by slightly modifying the usual arrangement of the memory system. In Fig. 10A, the respective memory chips comprise respectively a self-exciting oscillator which performs its own refreshing operation (self refreshing operation). For this reason, when a multiplicity of memory chips are employed, it is considered that some of the peak currents such as the peak currents i_1 and i_3 may be momentarily overlapped with each other. To avoid this, the values of the resistance R and capacitance C are set taking into consideration the overlapping of the three peak currents as the worst condition, that is, a sum thereof. Further, although the smoothing circuit comprising the elements C and R has been provided outside each of the memory LSI chips, it is also possible to previously provide the elements C and R within the each chip, in which case the area of the memory system can be decreased by an amount corresponding to the area occupied by the elements C and R.

Referring to Figs. 11A and 11B, there is shown another embodiment of the present invention which employs the smoothing circuit of Fig. 10A. The circuit of Fig. 11A includes a refreshing control circuit 1132, a refreshing operation activating signal generated from a power-cut-off detection signal or the like, an oscillator/timer 1128, a counter 1130, outputs ϕ_{refl} to ϕ_{refn} of the counter 1130 as memory refreshing control signals, and a memory section 1106. The memory section 1106 comprises memory chips M_1 to M_3 and smoothing circuits connected to respective power supply terminals of the respective memory chips M_1 to M_3. Fig. 10 shows the case where the memory chips comprise respectively a self-exciting oscillation circuit which performs its own re-

freshing operation (self refreshing operation). In this case, however, when the memory system is made to have a large capacity by providing a multiplicity of memory chips in the memory system, it is considered that, even when the peak currents are made smooth according to the foregoing embodiment, the peak currents of the many memory chips may be overlapped with each other, thus resulting in a large total peak current. To avoid this, the refreshing control signals ϕ_{refl} to ϕ_{refn} of the respective memory chips are controlled on a time sequential basis within the memory system as shown in Fig. 11B. As a result, in a sum i_t" of peak currents i_1 to i_n of the memory chips, no overlapping between the peak currents can be removed and thus any erroneous operation of the memory system due to a large current can be prevented.

Further, the memory system of the present embodiment may, for example, comprise a plurality of memory units each of which has 8 memory chips and which are activated by the aforementioned refreshing control signals ϕ_{refl} to ϕ_{refn}. As a result, the overlapping in the peak current between the memory units can be prevented. Thus, this method is required to control only the memory units, so that, even when the memory system has a large memory capacity, the number of refreshing control signals can be reduced, the refreshing control circuit can be simplified, and the refreshing control in a backup mode can be simplified.

The aforementioned oscillator/timer, the counter, etc. have known structures.

Fig. 12 is an example in which the smoothing circuits of Fig. 10 for reduction of the peak current level are applied to a portable file memory having a secondary battery as an auxiliary power supply. More particularly, Fig. 12 includes a memory system 1202 made in the form of a portable file memory and a reader/writer 1204 for performing reading and writing operations from and to the memory system. The memory system 1202 includes a power-off detection circuit 1216 for detecting such a power state as a power voltage drop or a power failure, a power detector 1218 provided in the power-off detection circuit 1216, a charging terminal 1222 for an auxiliary power supply 1212 (secondary battery), a charging circuit 1224 for the power supply 1212, a p-channel type MOS transistor Q_1, and a power-off detection signal OUT. Also provided in Fig. 12 are peak-current smoothing circuits as in Fig. 10A. In the power supply circuit in Fig. 10A, meanwhile, the switching from the main power supply 1010 to the auxiliary power supply 1012 has been automatically carried out on the basis of a voltage level difference between the main and auxiliary power supplies 1010 and 1012 through diodes D_1 and D_2 However, when the voltage level of the main power supply 1010 is 5 V and the auxiliary power supply 1012 in the form of a NiCd secondary battery has 4 cells each having an initial value of 1.35 to 1.4 V per one cell for example, the voltage level of the auxiliary power supply 1010 becomes 5.4-5.6 V. For this reason, a current supplied to the common power supply line V_{cc} in the normal operation allowing external access is not from the main power supply 1010 but from the auxiliary power supply 1012 which is higher in voltage level than the main 1010. For the purpose of preventing it, there is provided such an arrangement as shown in Fig. 12, wherein the p-channel MOS transistor Q_1 is provided in place of the diode D_2 in Fig. 10, the transistor is connected at its drain to the common power supply line V_{cc} and at its source to the auxiliary power supply 1212 so that, in such a backup operation as for a power voltage drop or a power off, the power-off detection signal OUT is used to set the gate terminal of the transistor at a low level to activate the transistor. In the normal operation, on the other hand, the power-off detection signal OUT is set at its high level to thereby inactivate the transistor, whereby the auxiliary power supply can be completely cut off in the normal operation. A diode D_3 in Fig. 12 is provided to prevent any reverse current during charging operation, and a resistance R_c is to control the charging current of the secondary battery. Since the backup auxiliary power supply 1212 has an initial voltage level of 5.6 V, a voltage higher than 5.6 V is applied to the charging terminal 1222. Accordingly, the charging power may be supplied from the reader/writer 1204 as illustrated in Fig. 12 or may be obtained from a boosting circuit provided within the memory system. It is also possible that, reversely, the voltage at the charging terminal can be used as the voltage of the memory chips and internal control circuit when reduced to 5 V.

The power-off detection circuit 1216 has a known structure and in particular, the power detector 1218 provided therein may comprise a comparator or the like.

Fig. 13 shows a practical detailed array of electronic parts used in a memory system 1302 of the present invention in the form of such a relatively small and portable file memory as a memory card. The illustrated 1302 includes auxiliary power sources for backup 1312a to 1312d, a power supply circuit 1308 for detecting a power-off state, inactivating memory chips and for switching between main and auxiliary power supplies, memory chips M_1 to M_4, a frame 1332 for the memory system 1302, a printed circuit board 1334 for mounting thereon the memory chips and other parts, and a control chip 1336 for selectively decoding the memory chips and for controllably mediating between the read/ write access operation and refreshing operation. Connected to the memory system 1302 is a connector 1338 for performing data input/output between the reader/writer 1204 and memory system 1302.

The electronic parts used in Fig. 13 can be mounted at a high density by making the electronic parts in the form of chips suitable for mounting on the board. For example, first capacities C and resistances R forming smoothing circuits can be mounted on the board at a high density. The capacities C are provided for the purpose of preventing the generation of high frequency noise caused by a large current. For example, the ca-

pacity C is wired in the vicinity of a power supply terminal of the memory chip M_3 to provide a shortest wiring between the power supply and grounding terminals, as represented by A. As a result, the inductance component of the power supply wiring can be minimized and therefore the object of removing the high frequency noise of the power supply can be effectively attained. The printed circuit board, for the purpose of avoiding internal and/or external noise, has a multi-layer structure comprising 3 or more layers, at least one of which is exclusively used mainly as a power supply line layer and in which power supply lines are made thick in line diameter to realize low resistance wiring of the power supply lines. Further, the resistance R is wired so as to provide a shortest wiring distance to a power supply terminal V_{cc} and to provide the minimized inductance component of the resistance R. With such an arrangement, the erroneous operation of the memory system 1302, which would be caused by the peak currents when dynamic memory chips are used for a small portable file memory system, can be suppressed. The second capacitance C_2 in Fig. 13 is provided to supply charges to the first capacitances C at the time of power change-over and to be operated at relatively low frequency. The capacitance C_2 can be located with a high degree of freedom. It goes without saying that it is necessary, in addition to the aforementioned capacitances, to provide to the power supply lines of the memory system 1302 a large-capacitance capacitor for removal of low frequency noise and a small-capacitance capacitor for removal of high frequency noise. Although explanation has been made mainly in connection with the memory circuit in the foregoing embodiment, the memory system of the present invention may be applied to memory LSI, logic LSI or other LSIs, so long as the memory system has a backup circuit based on battery and dynamic memory chips which can hold data at least partially therein through its own refreshing operation and can reduce the peak current level, or so long as the memory system has a circuit which can produce cyclically a peak current and can reduce the level of the peak current. In addition, the type of the battery used as the auxiliary power supply is not limited, in particular, and for such a memory LSI having a large consumption current as a dynamic memory, such a rechargeable type of battery as a secondary battery is convenient because it requires less frequent replacement.

The levels of the signals given in the foregoing embodiment are set to activate a predetermined circuit and thus the levels are not restricted to the illustrated high or low levels. Though the transistor Q_1 has comprised a p-channel transistor, the p-channel transistor may be used as an n-channel transistor if necessary by reversing the gate control of the transistor. Further, the portable memory system is supplied with power from a single power supply (battery) both in the normal operation and in the wait or backup operation, even in which case the present invention can advantageously reduce the peak current in the backup mode and lighten the burden of the battery to abruptly discharge a large current. As a result, there can be provided such a memory system that can reduce the level of a peak current for such an LSI chip as a dynamic memory in its wait operation mode and that can be suitably used for battery backup applications.

Another embodiment of the present invention is shown in Fig. 14, wherein Fig. 14A is a block diagram of a semiconductor memory system in accordance with the embodiment and Fig. 14B shows waveforms of a peak current in its normal and wait modes based on a refreshing operation. An LSI chip 1410 of Fig. 14A includes an X-direction address buffer 1414, a Y-direction address buffer 1416, a data input/output (I/O) buffer 1418, an X-direction decoder (XD) 1420, two memory arrays 1412a and 1412b divided by the X-direction decoder XD, Y-direction decoders (YD) 1422a and 1422b, a data input/ output signal line 1424, and a power supply terminal V_{CC}. The LSI chip 1412 further includes a controller 1426 for controlling a refreshing timer, an address counter and associated refreshing devices, an operational mode detecting means 1450, a refreshing control signal $\overline{REF}$ as an output of the means 1450, and a mode select signal 1438 which is generated at the refreshing controller 1426 on the basis of the control signal $\overline{REF}$ and according to the logic of a memory chip select signal and so on for switching between the wait and normal modes. In Fig. 14A, further, a word activation signal 1442 is used to switch to a different word line depending on the wait and normal operational modes, and an internal address signal 1440 is used to select either one of word lines of the X-direction decoder 1420. The LSI chip 1412 also includes a generator 1436 for generating the word activation signal 1442 in the wait mode, memory cells MC, n word lines W of the memory cells arranged in the X direction, a total m of bit lines B of the memory cells arranged in the Y direction at intervals of m/2 lines, a group of address signals A_{xi} in the X direction, a group of internal signals a_{xi} therefor, a group of address signals A_{yi}. in the Y direction, a group of internal signals a_{yi} therefor, and a group of input/output data I/O_i.

In Fig. 14B, on the other hand, reference numeral 1402 denotes a peak current flowing through the power supply terminal V_{cc} in the normal operational mode, 1404 a peak current in the wait operational mode, and 1406 a constant current component always flowing through the memory interior circuit as an activation current in the wait and normal operational modes.

In a usual dynamic memory, the resistance of word lines is a big problem causing the delay of an access time. For the purpose of avoiding this problem, the memory array is divided into two by the X-direction decoder (XD) 1420 as illustrated in Fig. 14A. Further, in order to reduce the resistance of the word lines and to enhance the speed thereby, the word lines are divided into a plurality of groups. In accordance with the present invention, by positively making most use of the memory cell

array necessarily determined by the division of the word lines, the reduction of the peak current can be achieved with a minor modification of the usual memory arrangement. Although explanation has been made as to the case where the operational mode detecting means 1450 is provided within the LSI chip in the present embodiment, such an $\overline{REF}$ input terminal as shown by a dotted line in Fig. 14A may be provided to enter as a signal a detection result detected by a means for detecting a power off (drop or increase in the power voltage) of an external electronic apparatus.

The operation of the present embodiment of the invention will then be explained by referring to Figs. 14A and 14B. In the refreshing operation based on the normal operational mode, the word lines at the both sides of the X-direction decoder (XD) 1420 are selected at the same time. As a result, the number of memory cells thus selected is m and the peak current I_p is proportional to the number m (= number of bit lines) of the selected memory cells. The constant current component 1406, which is very small compared with the peak current I_p, can be expressed as a relationship of $I_p \propto m$. In the wait operational mode based on the battery, the operational-mode switching signal 1438 to be applied to the X-direction decoder (XD) 1420 causes the number of cells connected to the word lines to be reduced to m/2. Accordingly, the peak current I_p in the wait operational mode is reduced to $I_p \propto m/2$.

A refreshing interval T_{c2} in the wait operational mode is made shorter than a refreshing interval T_{c1} in the normal operational mode and the frequency of the refreshing interval T_{c2} is made twice of that of the refreshing interval T_{c1} but this can be ignored because of now in the inactivation mode as already explained above.

As has been described in the foregoing, in the present invention, the mode switching signal 1438 is generated on the basis of the refreshing control signal REF received externally or from the operational-mode detecting means 1450 and according to the signal 1438, the plurality of word lines are switched. As a result, in the wait mode, the number of cells selected through one refreshing operation can be decreased and the refreshing interval can be correspondingly made narrow, thus resulting in that the peak current can be suppressed to a very low level.

Shown in Fig. 15A is a detailed example of the operational-mode detecting means 1450 in Fig. 14. That is, an operational-mode detecting means 1550 of Fig. 15A acts to detect a shift from the normal operational mode to the wait mode allowing holding of data and to output its detection result as the refreshing control signal REF having a level "1" or "0". In Fig. 15A, reference symbol V_{cc} denotes a power supply terminal and also a power voltage level on the terminal, V_R denotes a reference voltage for judgement of drop or increase in the power supply voltage internally generated or externally applied, and V_B the voltage of a backup battery. A discrimination circuit 1552 discriminates a high or low potential relation between the power supply voltage V_{cc} and reference voltage V_R as their inputs and outputs a low-level ("0") signal when the V_{cc} is higher than the V_R and outputs a high-level ("1") signal when the V_{cc} is lower therethan. An inverter circuit 1554 functions to invert the output signal of the discriminator 1552. The arrangement of this operational-mode detecting means 1550 is known and in particular, the discriminator 1552 may comprise a Schmitt trigger circuit or a comparison circuit.

As shown in Fig. 15B, the refreshing control signal $\overline{REF}$ is reduced to low level and activated when the power supply voltage V_{cc} drops to below the set reference voltage VR (= t_1), and the signal $\overline{REF}$ is increased to high level and inactivated when the voltage V_{cc} raises to above the reference level V_R (= t_2). Although one sort of level has been provided as the reference voltage V_R in the present embodiment, a plurality of levels of reference voltages V_R may be provided so that the refreshing control signal REF is easily activated and inactivated at the falling and rising times t_1 t_2 according to the drop and rise of the V_{cc} level. As such power-voltage-off (drop, rise) detecting circuit as mentioned above, many sorts of circuits have been proposed and one of such known circuits can be used as an operational mode detecting means to generate a switching signal in an operational mode, providing substantially the same effects.

Fig. 16 is a block diagram of a semiconductor memory system showing another embodiment of the present invention. In the drawing, reference numeral 1610 denotes an LSI chip, 1612-1 to 1612-k an array of memories, 1614 an X-direction address buffer, 1616 a Y-direction address buffer, 1618 a data input/output (I/O) buffer, 1620-1 to 1620-(k/2) X-direction decoders (XDs), 1644 logic circuits for selection of word lines, 1622-1 to 1622-k Y-direction decoder (YDs), and 1624 a data input/output signal line. In the drawing, further, numeral 1626 represents a controller for controlling a refreshing timer, an address counter and devices associated therewith, 1638 a mode select signal for switching between wait and normal operation modes, 1642 word line activation lines for switching the word lines of the wait and normal operation modes, 1636 a generator for producing the word line activation lines, and 1640 an internal address signal for selecting one of word lines at both sides of the X-direction decoder in the wait mode. In addition, reference symbol MC denotes a memory cell, W_{11} to W_{ik} (i x k) word lines of the memory cells arranged in the X direction, B_1 to B_m m bit lines of the memory cells arranged in the Y direction, A_{xi} a group of address signals for the X direction, a_{xi} internal signals for the X-direction address signals to be applied to the X decoders (XDs) 1620, A_{yi} a group of address signal for the Y direction, a_{yi} internal signals for the Y-direction address signal to be applied to the Y decoders (YDs) 1622, I/O_1 a group of input/output data, and $\overline{REF}$ a refreshing control sig-

nal.

Explanation will be made as to the refreshing operation of the present invention. In Fig. 16, in the refreshing operation in the normal operation mode, the word line activation signals 1642 as outputs of the signal generator 1636, which are all at high level, are applied to the logic circuits 1644 so that the k of the word lines W_{11} to W_{ik} in the Y direction are simultaneously selected through the logic circuits 1644 and are all set at high level, whereby a predetermined number of cells corresponding to m bits are refreshed. The next word lines W_{21} to W_{2k} are refreshed in the same manner. In the wait operational mode, on the other hand, under the control of the internal address signal 1640 issued from the controller 1626, the word line activation signals 1642 cause the X-direction word lines W_{11} to W_{ik}, i.e., W_{11}, W_{12}, ... to be separately activated. As a result, the number of cells (= number of bit lines) selected through one refreshing operation is reduced to m/k and the peak current in the refreshing operation is reduced to I/k.

The shift to wait operational mode at the time of battery backup is carried out based on the refreshing control signal $\overline{REF}$ in the present embodiment, but the shift may be easily realized by detecting the off state of the power supply voltage within the chip and generating the operational-mode switching signal as shown in Fig. 15A, whereby a semiconductor memory system having a good handleability can be obtained. In the present embodiment, explanation has been made in connection with the case where the address signal necessary for the refreshing operation in the wait mode is generated within the memory chip. However, even the address signal is applied from outside of the LSI chip, the same effect of reducing the value of the peak current as the above case can be obtained. It also goes without saying that, with respect to the division of the word lines in the refreshing operation of the wait operational mode, the number of activated word lines has been set to be equal to the physically divided number of the chip layout in the present embodiment, but such activated word line number may be arbitrarily set. In the latter case, the value of the peak current corresponds to tenths of the activated word line number arbitrarily set.

Further, although explanation has been directed mainly to the memory circuit in the foregoing embodiment, the present invention can be applied to all sorts of LSIs including memory LSI and logic LSI, so long as the LSI can hold data at least partially therein and be used for the purpose of reducing the value of the peak current in the wait mode from the normal mode, as has been already explained above. In addition, the aforementioned relationships of "0" and "1", and high and low levels may be reversed as necessary, in which case the logical relationship of the circuit are all reversed.

Accordingly, the value of the peak current of the LSI chip in the wait operational mode of the dynamic memory can be made highly small and there can be provided a semiconductor memory system which is suitable for battery backup.

Prior to the description of another embodiment of the present invention with reference to Fig. 17, consideration will be directed to the embodiment of the memory card explained in connection with Figs. 3 and 4.

When the connector 310 is not connected to such a data processor as a computer, power is supplied from the backup battery 311 through the power switching circuit 312 to the PSRAM 320 so that the self refreshing circuit 320a incorporated in the PSRAM 320 is operated and the PSRAM 320 performs its refreshing operation. This causes data to be held in the PSRAM 320, eliminating the need for any external refreshing operation. When the connector 310 is connected to the data processor, on the other hand, power is supplied from the data processor through the connector 310, power supply line 310a and power switching circuit 312 to the PSRAM 320. In this case, the refreshing request signal for the PSRAM 320 is generated at the access control circuit 319.

Since the refreshing operation can be carried out within the memory card independently of the external data processor in this manner, the data processor is required to perform only the similar control operation to the memory card having the SRAM and thus the present memory card can have a compatibility with the SRAM memory card.

When it is desired to store in the memory card the data of the data processor connected to the connector 310, the address signal is supplied from the data processor through the connector 310 and address signal line 310b to the address buffer 315 to specify the write address of the PSRAM 320. At the same time, the write enable signal $\overline{WE}$ is supplied from the data processor through the control signal line 310c to the access controller 319 and a data is supplied from the data processor through the data signal line 310d and data buffer 316 to the PSRAM 320 to write the supplied data in the specified address of the PSRAM 320.

When it is desired to read out a data from the PSRAM 320, similarly, the address signal through the address signal line 310b and the control signals such as the chip enable signal $\overline{CE}$ and output enable signal $\overline{OE}$ through the control line 310c are supplied to the PSRAM 320, so that a data is read out from the address of the PSRAM specified by the address signal and supplied therefrom through the data buffer 316, data signal line 310d and connector 310 to the data processor.

In the data reading operation, the access controller 319, when receiving the decoded output of the address signal from the decoder 314 and receiving the signal $\overline{CE}$ through the control signal line 310c, is operated to cause the data reading operation of the PSRAM 320 but to also control to avoid the overlapping between the data reading and refreshing operations because the refreshing request signal is also generated to cause the refreshing operation of the PSRAM 320.

The decoder 314 may be provided between the ac-

cess controller 319 and the PSRAM 320 so that the access controller 319 is operated in response to the signal $\overline{CE}$ and the decoder 314 is operated in response to the output of the access controller 319. Further, when the PSRAM array is provided only one, the decoder 314 may be removed.

In Fig. 4 showing the detailed example of the access controller 319 in Fig. 3, the access controller 319 comprises the access arbitration circuit 419a and the chip enable signal conversion circuit 419b.

The access arbitration circuit 419a includes a first circuit in which the R-S flip-flop comprises the NAND gates 406a and 406b and an output of the NAND gate 406a is delayed through the delay 405a and then fed back to the NAND gate 406b, and a second circuit in which an output of the NAND gate 406b is delayed through the delay 405b and then fed back to the NAND gate 406a. In the access arbitration circuit 419a, the signal $\overline{CE}$ is inverted with respect to level and then applied to the NAND gate 406a, while the refreshing request signal $\overline{RFSH}$ is applied from the refreshing timer 419c to the NAND gate 406b. The output of the NAND gate 406a is the read access enable signal $\overline{Access}$ which enables the read access to the PSRAM 320, while the output of the NAND gate 406b is the refreshing enable signal $\overline{Refresh}$ which enables the refreshing operation of the PSRAM 320.

With such an arrangement, when the refreshing request signal $\overline{RFSH}$ and the signal $\overline{CE}$ are supplied, the refreshing enable signal $\overline{Refresh}$ is generated at the same timing as the refreshing request signal $\overline{RFSH}$ in such a time duration as shown by ① in Fig. 17 but the read access enable signal $\overline{Access}$ is generated as delayed from the tailing edge of the refreshing request signal $\overline{RFSH}$ by a delay time τ_b of the delay circuit 405b. Thus, the PSRAM 320 performs its data reading operation after the delay time τ_b from the completion of the refreshing operation in such a time duration as shown by ② in Fig. 17.

When the refreshing request signal $\overline{RFSH}$ is generated during the active (generation) duration of the signal $\overline{CE}$, the refreshing enable signal $\overline{Refresh}$ is generated after a delay time τ_a of the delay circuit 405a from the completion of the signal $\overline{CE}$ and read access enable signal $\overline{Access}$, in such a time duration as shown by ③ in Fig. 17. Thus, the PSRAM 320 performs its refreshing operation after the delay time τ_a from the completion of the data reading operation.

The refreshing timer 419c is reset by an output signal of the delay circuit 405a so that, even when the refreshing request signal $\overline{RFSH}$ is generated at any timing, the time width of the refreshing enable signal $\overline{Refresh}$ can be made constant.

In the chip enable signal conversion circuit 419b in Fig. 4, the EXOR circuits 402a, 402b, ..., and 402n detect a time point at the time of a change in the address signal and supply pulse signals indicative of the change time point and the signal $\overline{CE}$ to the OR circuit 403, whereby the signal $\overline{CE_p}$ corresponding to the signal $\overline{CE}$ indicative of the address change time points, as shown in Fig. 18. The signal CE_p is applied to the AND gate 404 together with a gate signal corresponding to the inversion of the read access enable signal $\overline{Access}$ and then supplied to the chip enable terminal $\overline{CE}$ of the PSRAM 320.

Meanwhile, the PSRAM 320 reads out therefrom a data corresponding to the then specified address after a predetermined read access time from the rising edge of the signal $\overline{CE_p}$ and also operates the data buffer 316 at this timing to transfer the read-out data therefrom through the data buffer 316 to the data processor.

Fig. 19 is a block diagram of another embodiment of the semiconductor memory system in accordance with the present invention, which includes a delay circuit 1907, an inverter 1908, an OR circuit 1909 and a latch circuit 1916a.

In the drawing, the delay circuit 1907 for providing a delay to an output of the NAND gate 1906a, the inverter 1908 for inverting the output level of the delay circuit 1907, and the OR circuit 1909 for receiving outputs of the NAND gate 1906a and inverter 1908 are provided between an NAND gate 1906a and a delay circuit 1905a to latch the data read out from the PSRAM 320.

An OR circuit in Fig. 19 outputs a signal corresponding to the signal $\overline{CE}$ attached with pulses indicative of the change time points in the address signal, which output signal is applied to the R-S flip-flop. The refreshing enable signal $\overline{Refresh}$ is output from an NAND gate 1906b, while the read access enable signal $\overline{Access}$ is output from the OR circuit 1909. This read access enable signal $\overline{Access}$ is generated from the OR circuit 1909 based on its logic sum operation. More in detail, an output of the NAND gate 1906a is applied to the OR circuit 1908 and is also delayed at the delay circuit 1907 and inverted at the inverter 1908 to obtain an inverted signal. The inverted signal from the inverter is applied also to the OR circuit 1909 to perform its logic sum operation of the output of the NAND gate 1906a and the inverted signal. The signal Access is an "L" level signal which has a time width equal to a delay time τ_c of the delay circuit 1907.

The operation of the present embodiment will next be explained, for the brevity of explanation, by referring to Fig. 20 in connection with the case where the output of the OR circuit 1903 is the signal $\overline{CE}$ itself, the signal $\overline{CE}$ is generated in the active (generation) duration of the refreshing request signal $\overline{RFSH}$, and the next refreshing request signal $\overline{RFSH}$ is generated in the generation duration of the signal $\overline{CE}$.

When the refreshing request signal $\overline{RFSH}$ is generated and the signal $\overline{CE}$ is supplied during the generation of the signal RFSH to instruct the read access mode, an output of the NAND gate 1906b as well as a signal corresponding to the same output delayed by the delay time τ_b cause through a delay circuit 1905b are applied to the NAND gate 1906a, so that the NAND gate

1906a is turned OFF not to output the signal $\overline{\text{CE}}$ therefrom. The output of the NAND gate 1906b corresponds to the refreshing enable signal $\overline{\text{Refresh}}$.

When the refreshing request signal $\overline{\text{RFSH}}$ is terminated and the delay time τ_b of the delay circuit 1905b elapses, the NAND gate 1906a outputs the signal $\overline{\text{CE}}$ and at this timing, the OR circuit 1909 outputs the read access enable signal $\overline{\text{Access}}$ having a time width equal to the delay time τ_c of the delay circuit 1907.

When this results in that the PSRAM is subjected by the refreshing enable signal $\overline{\text{REFRESH}}$ to a refreshing operaiton, the PSRAM is subjected by the read access enable signal Access to a read accessing operation and a data reading operation therefrom after the delay time τ_c from the completion of the refreshing operation.

At this time, the data read out from the PSRAM is supplied to a data buffer 1916 and latched at the trailing edge (rising edge) of the read access enable signal $\overline{\text{Access}}$.

Next, when the next refreshing request signal $\overline{\text{RFSH}}$ is generated in the read access mode based on the signal $\overline{\text{CE}}$, since the output of the signal from the OR circuit 1909 is already completed, the refreshing request signal $\overline{\text{RFSH}}$ is output from the NAND gate 1906b as the refreshing enable signal $\overline{\text{Refresh}}$ to carry out the refreshing operation of the PSRAM.

Even when the signal $\overline{\text{CE}}$ from the external data processor causes the read access mode of the PSRAM to be specified and the read access mode lasts long to generate the refreshing request signal $\overline{\text{RFSH}}$ in this mode in this way, the read access mode of the PSRAM is prescribed actually by the read access enable signal $\overline{\text{Access}}$ having the time width τ_c issued from the OR circuit 1909, which results in that the PSRAM is subjected to a refreshing operation in response to this refreshing request. At this time, since the data read out from the PSRAM is latched at the latch circuit 1916a of the data buffer 1916, this will not cause any trouble in the data reading operation of the data processor.

It goes without saying that, when the refreshing request signal $\overline{\text{RFSH}}$ is generated during the output of the read access enable signal $\overline{\text{Access}}$ from the OR circuit 1909, the refreshing enable signal $\overline{\text{Refresh}}$ is generated after the delay time τ_a of the delay circuit 1905a from the completion of the read access enable signal $\overline{\text{Access}}$.

Shown in Fig. 21 is a block diagram of a semiconductor memory control system in accordance with another embodiment of the present invention, which includes a frequency divider 2121, a flip-flop 2122, inverters 2123 and 2124, NAND gates 2125 and 2126, an OR circuit 2127, a NOR circuit 2128, and D flip-flops 2129, 2130 and 2131.

Explanation will then be made as to the operation of the present embodiment by referring to Figs. 22A, 22B and 22C.

Referring first to Fig. 21 and 22A, the frequency divider 2121 outputs a pulse from its terminal Q_n at intervals of n pulses in a clock signal CLK, while the flip-flop 2122 generates at its terminal Q_1 a Q_1 output whose level is inverted and a Q_2 output corresponding to 1/2 of the frequency of the Q_1 output each time receiving an output pulse from the frequency divider 2121. These frequency divider 2121 and the flip-flop 2122 make up a counter which counts the clock CLK.

The signal $\overline{\text{CE}}$ from the data processor (not shown) is shaped at the D flip-flop 2129 whose falling and rising edges are synchronized with the clock signal CLK, supplied to the NOR circuit 2128 and added thereat to a signal ATD indicative of a change time point in the address signal generated as in the chip enable signal conversion circuit 419b of Fig. 4 to thereby form a signal ϕ_R added with pulses corresponding to the change time points in the address signal.

In a standby mode shown in Fig. 22B, the signal $\overline{\text{CE}}$ supplied to the D flip-flop 2129 is at level "H" while the signal ϕ_R issued from the NOR circuit 2128 is kept at level "L".

The Q_1 output of the flip-flop 2122 is inverted with respect to level at the inverter 2123, whereas the Q_2 output of the flip-flop 2122 is supplied directly to the NAND gate 2125. Accordingly, the NAND gate 2125 outputs the refreshing request signal $\overline{\text{RFSH}}$ of level "L" only for the former half of the "H" duration of the Q_2 output of the flip-flop 2122, which signal $\overline{\text{RFSH}}$ is used as the refreshing enable signal (not shown) for the PSRAM. Thus, the PSRAM is refreshed in every "L" duration of the refreshing request signal $\overline{\text{RFSH}}$.

The Q_1 output level-inverted at the inverter 2123 and the Q_2 output level-inverted at the inverter 2124 are applied to the NAND gate 2126 which in turn outputs such a signal that has level "L" in the former half of the "L" duration of the Q_2 output, in which case the D fllip-flop 2123 is in its reset released state. Therefore, in the D flip-flop 2131, its input D is sample-held at the initial falling edge of the output of the AND gate 2126 and its output Q is kept at level "H". And when the output of the NAND gate 2126 and the output Q of the D flip-flop 2123 held at level "H" are applied to the OR circuit 2127, the read access enable signal $\overline{\text{Access}}$ issued from the OR circuit 2127 is kept at level "H". As a result, the PSRAM is inhibited from being subjected to a read accessing operation.

In this manner, in the standby mode, the PSRAM is cyclically subjected to flip-flop operation at a constant period.

When it is desired to read out a data from the PSRAM as shown in Fig. 22C, the signal $\overline{\text{CE}}$ is set at level "L" to instruct the read access mode from the data processor.

When attention is directed to an initial duration of the signal $\overline{\text{CE}}$ having level "L" in a duration shown by 1 in Fig. 22c, the signal ϕ_R issued from the NOR circuit 2128 is synchronized with the clock CLK and corresponds to the level inversion of the signal $\overline{\text{CE}}$ in the absence of the signal ATD. For this reason, in the "H" du-

ration of the signal ϕ_R, i.e., in the "L" duration of the signal $\overline{CE}$, the D flip-flop 2131 is in its reset released state.

When the output of the NAND gate 2126 is initially at level "L", the D flip-flop 2131 still remains in its reset released state and has the Q output of level "L", so that the read access enable signal $\overline{\text{Access}}$ as the output of the OR circuit 2127 is at level "L", during which the PSRAM is subjected to a data reading operation therefrom. A data read out from the PSRAM is supplied to the latch circuit 2116 and latched therein at the rising edge (trailing edge) of the read access enable signal $\overline{\text{Access}}$.

Meanwhile, the D flip-flop 2131 samples and holds the D input of its terminal D having level "H" at the initial rising edge of the output of the NAND gate 2126 after its reset release to provide level "H" to the Q output at its output terminal Q. This continues until the output signal ϕ_R of the NOR circuit 2128 is changed to level "L", that is, until the signal $\overline{CE}$ is changed to level "H" and the D flip-flop 2131 is reset.

Under such a condition, when there is no change in the address signal and data reading is carried out from the specified address of the PSRAM during the duration of the read access mode specified by the signal $\overline{CE}$, the D flip-flop 2131 masks the "L" duration in the output of the NAND gate 2126 to inhibit the output of the OR circuit 2127 and thereby prevent thereafter the read re-access during the specified read access mode duration.

Assume next that the read access mode is again specified by the signal $\overline{CE}$ during the "L" duration of the Q_2 output of the flip-flop 2122 in such a duration as denoted by ② in Fig. 22C.

In this case, the D flip-flop 2130 samples and holds the Q_2 output of level "L" at the rising edge of the signal ϕ_R from the NOR circuit 2128 and provides level "L" to its q output, whereby the flip-flop 2122 is reset at the falling edge of the Q output, from which timing the counter comprising the frequency divider 2121 and the flip-flop 2122 restarts the counting operation of the clock signal CLK. Thus, from the reset timing of the flip-flop 2122, the Q_1 output of the flip-flop 2122 is at level "L" for a time duration corresponding to 1/2 of the period of the Q_1 output and the Q_2 output thereof is also at level "L" for a time duration corresponding to 1/2 of the period of the Q_2. During the duration of the "L" level of the both Q_1 and Q_2 outputs (which duration starts from the rising edge of the signal ϕ_R), the output of the NAND gate 2126 becomes level "L" and the reset state of the D flip-flop 2131 is released at the rising edge of the signal ϕ_R. As a result, the signal ϕ_R has level "H" and the read access enable signal $\overline{\text{Access}}$ from the OR circuit 2127 has level "L", whereby the reading operation of the PSRAM is carried out. Thereafter, the same operation as explained in connection with the duration 1 in Fig. 22C is carried out.

In this manner, through the masking function of the D flip-flop 2131, only one data reading operation is ensured for the specified address and the refreshing operation of the PSRAM is carried out without any break during the period where no read access is effected.

In the present embodiment, since the data read out through the read access operation is latched at the latch circuit 2116a at the end of the reading operation, the refreshing operation of the PSRAM can be realized without any troubles and it can be avoided that the input of the read data to the data processor is influenced by the refreshing operation of the PSRAM.

Further, since the read data is latched to put the PSRAM in its standby mode, power saving can be realized. In addition, according to the present embodiment, the refreshing operation of the PSRAM can be periodically realized regardless of the time duration length of the external read access mode to ensure the data holding of the PSRAM, the data can be prevented from being destroyed by the refreshing operation, and the output of the read data to the external device can be achieved without any troubles.

Claims

1. A semiconductor memory apparatus comprising:

   a dynamic RAM (320, 801) which conducts a refresh operation in response to a refresh enable signal (REFRESH) and is accessible in response to an access enable signal (ACCESS) internal refresh means (320a; 419c; 807,808) connected to said dynamic RAM for generating an internal refresh signal indicating an internal refresh operation of the dynamic RAM;
   signal reception means (310) for receiving an memory access signal (CE) from an external device for access to said semiconductor memory apparatus; and
   access control means (319) for controlling access to and refresh operations of the dynamic RAM; characterised in that:
   said access control means includes counter means (621) for counting a clock signal (CLOCK) supplied from either the external device or a clock generation circuit (318) of said semiconductor memory apparatus and logic operation means (623, 624) for performing a logic operation of said memory access signal (CE) and an output signal (Q_n,Q_{n-1}) of said counter means (621); wherein at least two bits in a count value of said counter means are allocated to four periods comprising: a period allowing generation of said access enable signal (ACCESS); a precharge period for said access enable signal; a period for allowing generation of said refresh enable signal (REFRESH); and a precharge period for said refresh enable signal, which periods occur in sequence with said clock signal, and wherein said access control means (319) generates said refresh enable signal (REFRESH) when values of said two digit

bits are those allocated to said period for generating said refreshe enable signal (REFRESH) and said access control means (319) generates said access enable signal (ACCESS) when said memory access signal (CE) is received during a time period when the values of the two digit bits are those allocated to said period for generating the access enable signal (ACCESS) (Fig. 6,7).

2. A semiconductor memory apparatus according to claim 1, wherein said memory access signal (CE) is a read access signal and said access enable signal (ACCESS) lasts for a predetermined read access time period and wherein said semiconductor memory apparatus further comprises latch means (1916a) for latching data read out of said dynamic RAM at completion of said read access time period.

3. A semiconductor memory apparatus according to claim 1, wherein said access control means (319) comprises address change detection means (419b) for detecting a change in an address signal supplied from the external device; and wherein said access control means generates, when said address change detection means detects a change in said address signal when caused by reading data, a DRAM read signal (CE_p) corresponding to logic level inversion of said memory access signal (CE) for a predetermined period.

4. A semiconductor apparatus according to claim 3, wherein said memory access signal includes a memory chip select signal and a chip enable signal (CE).

5. A semiconductor memory apparatus according to claim 1, 2, 3 or 4, further comprising battery means (311) for supplying power to said dynamic RAM and a power supply switching circuit (312) connected to said battery means and said signal reception means (310) for, when said semiconductor memory apparatus is mounted to the external device, supplying power to the dynamic RAM not from said battery means but from the external device.

Patentansprüche

1. Halbleiter-Speichereinrichtung, umfassend

einen dynamischen RAM (320, 801), der bei Auftreten eines Aktualisier-Freigabesignals (REFRESH) einen Aktualisiervorgang durchführt und bei Auftreten eines Zugriffs-Freigabesignals (ACCESS) Zugriff gestattet,
eine an den dynamischen RAM angeschlossene interne Aktualisiereinrichtung (320a; 419c; 807, 808) zur Erzeugung eines internen Aktualisiersignals, das einen internen Aktualisiervorgang des dynamischen RAM angibt,
eine Signalempfangseinrichtung (310) zum Empfang eines Speicherzugriffssignals (CE) von einem externen Gerät für den Zugriff auf die Halbleiter-Speichereinrichtung, und
eine Zugriffssteuereinrichtung (319) zur Steuerung des Zugriffs auf den dynamischen RAM sowie zur Steuerung von dessen Aktualisiervorgängen,

dadurch **gekennzeichnet,** daß die Zugriffssteuereinrichtung eine Zähleranordnung (621) zum Zählen eines entweder von dem externen Gerät oder von einer Taktgeneratorschaltung (318) der Halbleiter-Speichereinrichtung zugeführten Taktsignals (CLOCK) sowie eine Logik-Operationseinrichtung (623, 624) zur Durchführung einer logischen Operation an dem Speicherzugriffssignal (CE) und einem Ausgangssignal (Q_n, Q_{n-1}) der Zähleranordnung (621) umfaßt; wobei mindestens zwei Bits in einem Zählwert der Zähleranordnung vier Perioden zugeordnet sind, zu denen eine Periode, die die Erzeugung des Zugriffs-Freigabesignals (ACCESS) gestattet, eine Vorladeperiode für das Zugriffs-Freigabesignal, eine Periode, die die Erzeugung des Aktualisier-Freigabesignals ((REFRESH) gestattet, und eine Vorladeperiode für das Aktualisier-Freigabesignal gehören, wobei die Perioden mit dem Taktsignal sequentiell auftreten, und wobei die Zugriffssteuereinrichtung (319) das Aktualisier-Freigabesignal (REFRESH) erzeugt, wenn Werte der genannten zwei Bitstellen die der Periode zur Erzeugung des Aktualisier-Freigabesignals (REFRESH) zugeordneten sind, und die Zugriffssteuereinrichtung (319) das Zugriffs-Freigabesignal (ACCESS) erzeugt, wenn das Speicherzugriffssignal (CE) während einer Zeitperiode empfangen wird, zu der die Werte der beiden Bitstellen die der Periode zur Erzeugung des Zugriffs-Freigabesignals (ACCESS) zugeordneten sind (Fig. 6, 7).

2. Halbleiter-Speichereinrichtung nach Anspruch 1, wobei das Speicherzugriffssignal (CE) ein Lesezugriffssignal ist und das Zugriffs-Freigabesignal (ACCESS) während einer vorgegebenen Lese-Zugriffszeit andauert, und wobei die Halbleiter-Speichereinrichtung ferner eine Zwischenspeichereinrichtung (1916a) umfaßt, um aus dem dynamischen RAM ausgelesene Daten nach Beendigung der Lesezugriffs-Zeitspanne zwischenzuspeichern.

3. Halbleiter-Speichereinrichtung nach Anspruch 1, wobei die Zugriffssteuereinrichtung (319) eine Adreßänderungs-Erfassungseinrichtung (419b) zur Erfassung einer Änderung in einem von dem externen Gerät zugeführten Adressensignal ermittelt;

und wobei die Zugriffssteuereinrichtung dann, wenn die Adreßänderungs-Erfassungseinrichtung eine Änderung in dem Adressensignal, sofern durch das Lesen von Daten verursacht, ermittelt, ein DRAM-Lesesignal (E_p) erzeugt, das einer Umkehr des logischen Pegels des Speicherzugriffssignals (CE) während einer vorgegebenen Periode entspricht.

4. Halbleiter-Speichereinrichtung nach Anspruch 3, wobei das Speicherzugriffssignal ein Speicherchip-Auswahlsignal und ein Chip-Freigabesignal (CE) enthält.

5. Halbleiter-Speichereinrichtung nach einem der Ansprüche 1 bis 4, mit einer Batterieanordnung (311) zur Energieversorgung des dynamischen RAM und einer mit der Batterieanordnung und der Signalempfangseinrichtung (310) verbundenen Energieversorgungs-Schaltstufe, die dann, wenn die Halbleiter-Speichereinrichtung an dem externen Gerät montiert ist, den dynamischen RAM nicht aus der Batterieeinrichtung sondern aus dem externen Gerät mit Energie versorgt.

Revendications

1. Dispositif de mémoire à semi-conducteurs comprenant:

   une RAM dynamique (320, 801) qui exécute une opération de rafraîchissement en réponse à un signal d'activation de rafraîchissement (REFRESH) et est accessible en réponse à un signal d'activation d'accès (ACCESS),
   un moyen de rafraîchissement interne (320; 419C; 807, 808) connecté à ladite RAM dynamique pour générer un signal de rafraîchissement interne indiquant une opération de rafraîchissement interne de la RAM dynamique;
   un moyen (310) de réception de signal destiné à recevoir un signal (CE) d'accès de mémoire en provenance d'un dispositif extérieur pour accéder audit dispositif de mémoire à semi-conducteurs; et
   une moyen (319) de commande d'accès destiné à commander l'accès à la RAM dynamique et les opérations de rafraîchissement de cette RAM dynamique; caractérisé en ce que:
   ledit moyen de commande d'accès comprend un moyen formant compteur (621) destiné à compter un signal d'horloge (CLOCK) fourni à partir soit du dispositif extérieur, soit d'un circuit (318) de génération d'horloge dudit dispositif de mémoire à semi-conducteurs et des moyens logiques (623, 624) pour effectuer une opération logique dudit signal (CE) d'accès de mémoire et un signal de sortie (Qn, Qn-1) dudit moyen formant compteur (621); dans lequel au moins deux bits dans une valeur de compte dudit moyen formant compteur sont assignés à quatre périodes comprenant: un période permettant la génération dudit signal d'activation d'accès (ACCESS); une période de chargement préalable pour ledit signal d'activation d'accès; une période pour permettre la génération dudit signal d'activation de rafraîchissement (REFRESH) et une période de chargement préalable pour ledit signal d'activation de rafraîchissement, ces périodes ayant lieu en séquence avec ledit signal d'horloge, et dans lequel ledit moyen (319) de commande d'accès génère ledit signal d'activation de rafraîchissement (REFRESH) quand les valeurs des deux bits précités sont celles assignées à ladite période de génération dudit signal d'activation de rafraîchissement (REFRESH) et ledit moyen (319) de commande d'accès génère ledit signal d'activation d'accès (ACCESS) quand ledit signal (CE) d'accès de mémoire est reçu pendant une période de temps durant laquelle les valeurs des deux bits sont celles assignées à ladite période de génération de signal d'activation d'accès (ACCESS) (Fig. 6, 7).

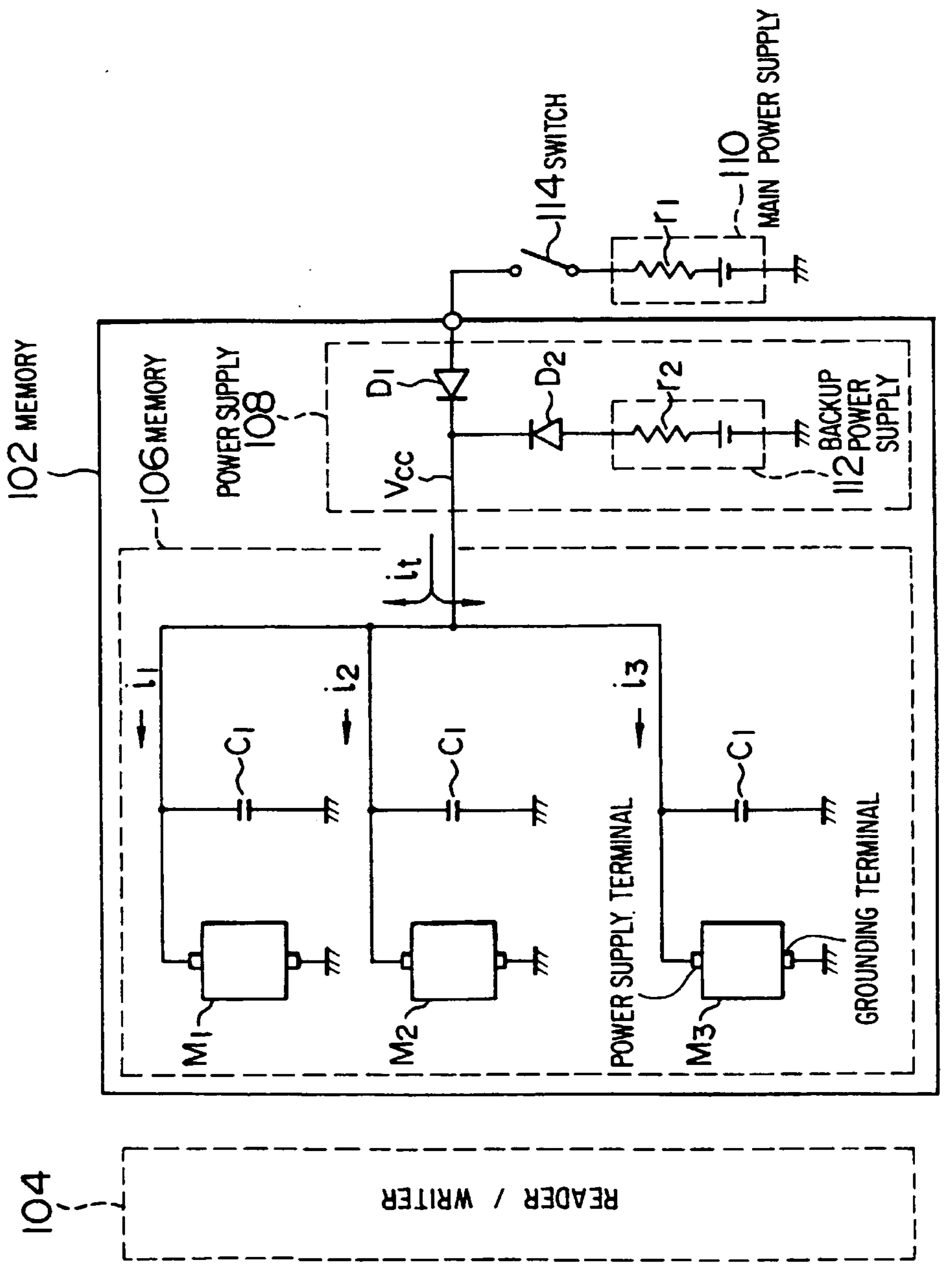
2. Dispositif de mémoire à semi-conducteurs selon la revendication 1, dans lequel ledit signal (CE) d'accès de mémoire est un signal d'accès de lecture et ledit signal d'activation d'accès (ACCESS) dure pendant une période prédéterminée de temps d'accès de lecture et dans lequel ledit dispositif de mémoire à semi-conducteurs comprend, en outre, un moyen formant verrou (1916a) pour verrouiller les données extraites de ladite RAM dynamique à la fin de ladite période de temps d'accès de lecture.

3. Dispositif de mémoire à semi-conducteurs selon la revendication 1, dans lequel ledit moyen (319) de commande d'accès comprend un moyen (419b) de détection de changement d'adresse pour détecter un changement dans un signal d'adresse fourni à partir du dispositif extérieur; et dans lequel ledit moyen de commande d'accès génère, quand ledit moyen de détection de changement d'adresse détecte un changement dans ledit signal d'adresse lorsqu'il est provoqué par les données de lecture, un signal (Ep) de lecture de DRAM correspondant à une inversion de niveau logique dudit signal (CE) d'accès de mémoire pendant une période de temps prédéterminée.

4. Dispositif de mémoire à semi-conducteurs selon la revendication 3, dans lequel ledit signal d'accès de mémoire comprend un signal de sélection de circuit de mémoire et un signal (CE) d'activation de circuit.

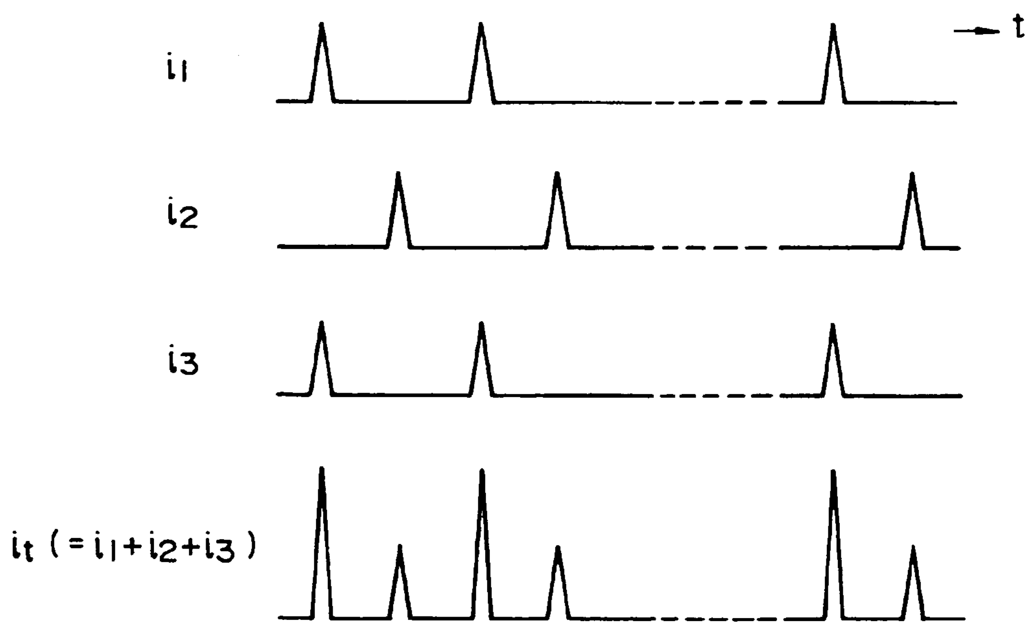
5. Dispositif de mémoire à semi-conducteurs selon la revendication 1, 2, 3 ou 4, comprenant, en outre, un moyen formant batterie (311) pour fournir de l'énergie à la RAM dynamique et un circuit (312) de commutation d'alimentation connecté audit moyen formant batterie et audit moyen (310) de réception de signal pour que, lorsque le dispositif de mémoire à semi-conducteurs est relié audit dispositif extérieur, l'énergie soit fournie à la RAM dynamique non pas à partir de la batterie mais à partir du dispositif extérieur.

FIG. 1A


102 MEMORY
106 MEMORY
POWER SUPPLY 108
114 SWITCH
r1
110 MAIN POWER SUPPLY
D1
D2
r2
112 BACKUP POWER SUPPLY
Vcc
it
i1
i2
i3
C1
C1
C1
M1
M2
M3
POWER SUPPLY TERMINAL
GROUNDING TERMINAL
104
READER / WRITER

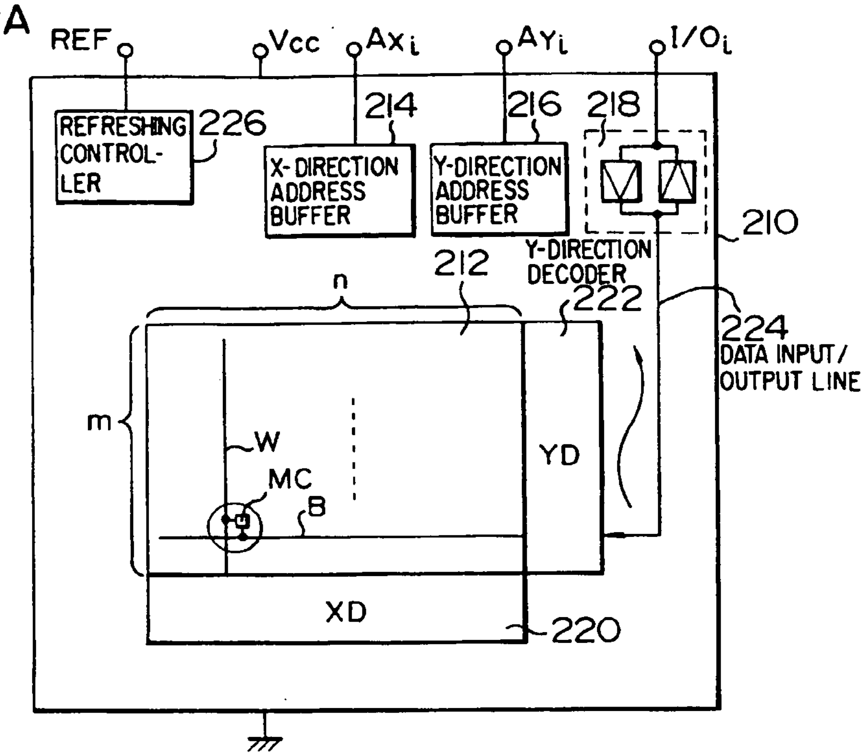
EP 0 425 693 B1

F I G. 1B



EP 0 425 693 B1

F I G. 2A



F I G. 2B

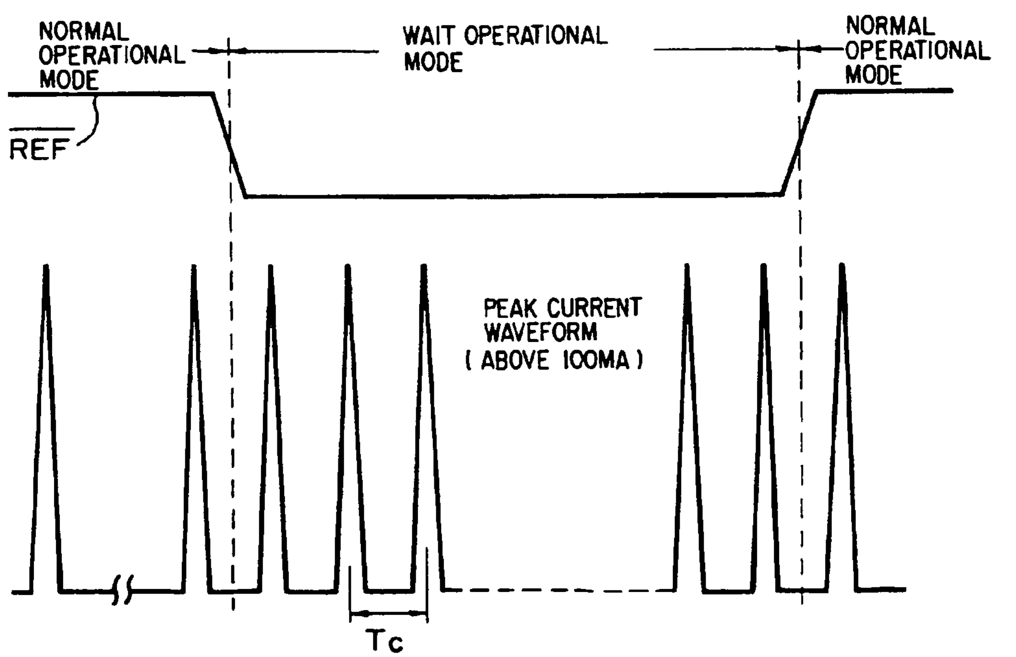
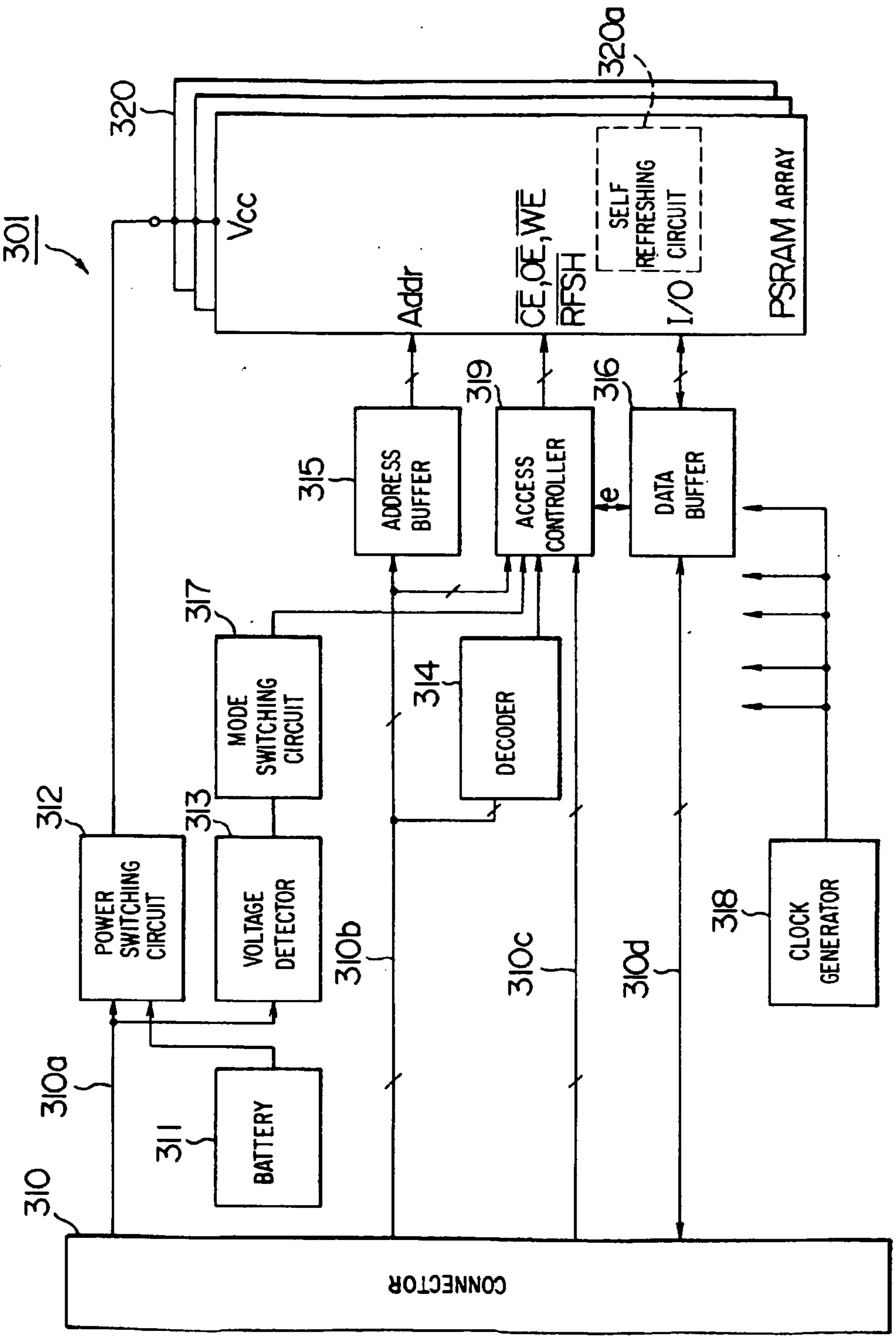


FIG. 3


301
320
320a
Vcc
SELF REFRESHING CIRCUIT
PSRAM ARRAY
Addr
CE, OE, WE
RFSH
I/O
315
ADDRESS BUFFER
319
ACCESS CONTROLLER
e
316
DATA BUFFER
317
MODE SWITCHING CIRCUIT
314
DECODER
312
POWER SWITCHING CIRCUIT
313
VOLTAGE DETECTOR
310b
310c
310d
318
CLOCK GENERATOR
310a
311
BATTERY
310
CONNECTOR

F I G. 4

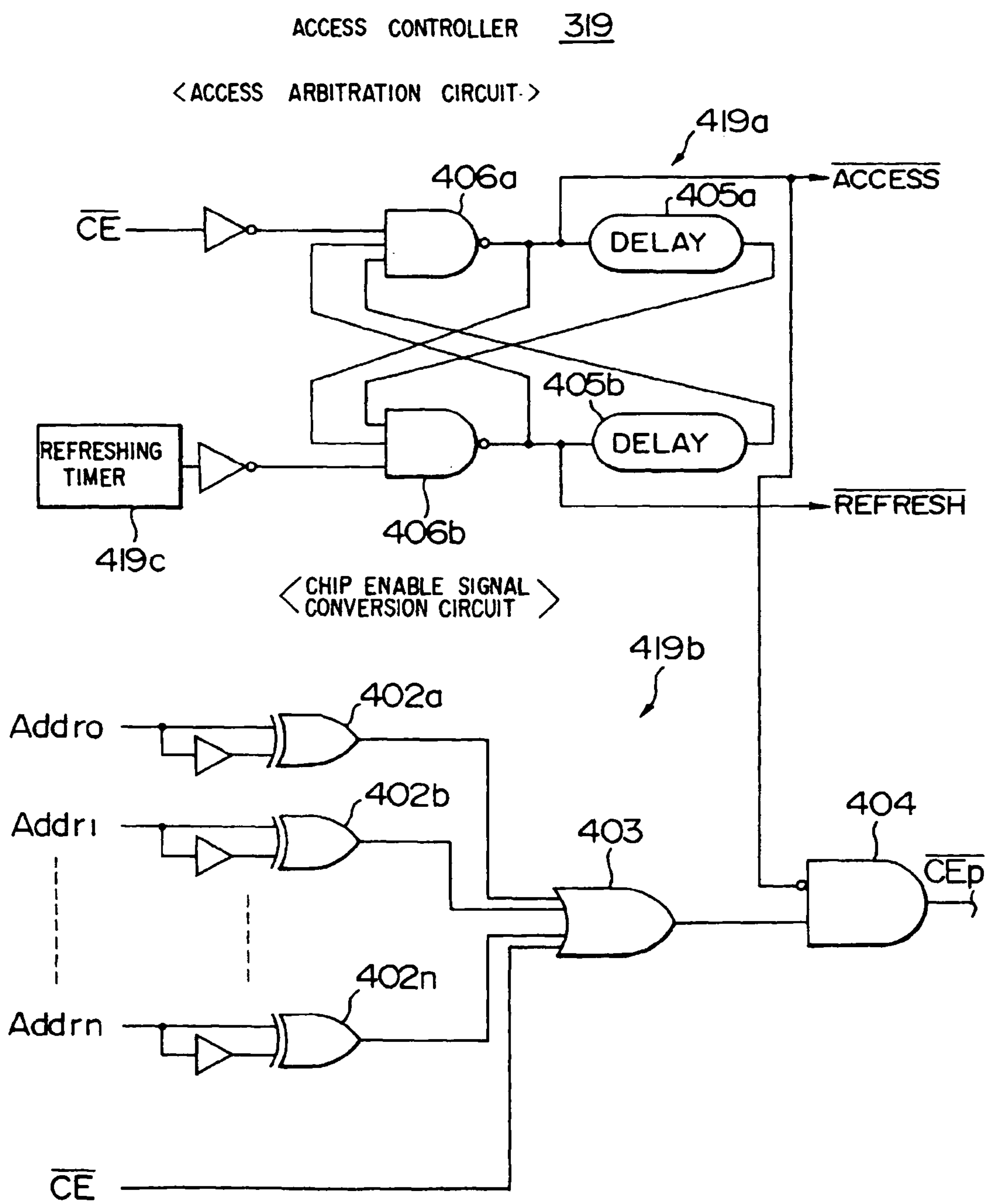

ACCESS CONTROLLER 319
<ACCESS ARBITRATION CIRCUIT>
419a
406a
405a
ACCESS
CE
DELAY
405b
REFRESHING TIMER
DELAY
406b
REFRESH
419c
<CHIP ENABLE SIGNAL CONVERSION CIRCUIT>
419b
402a
Addro
402b
Addr1
403
404
CEp
402n
Addrn
CE

FIG. 5A

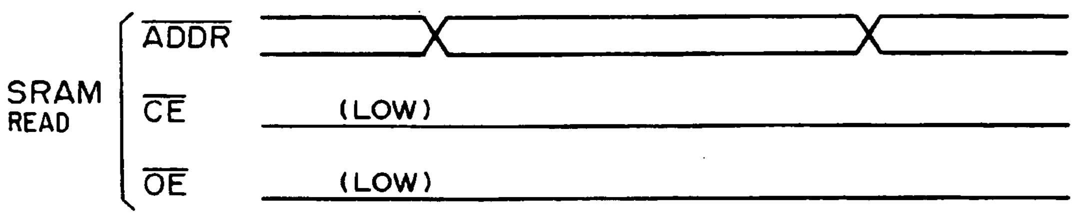
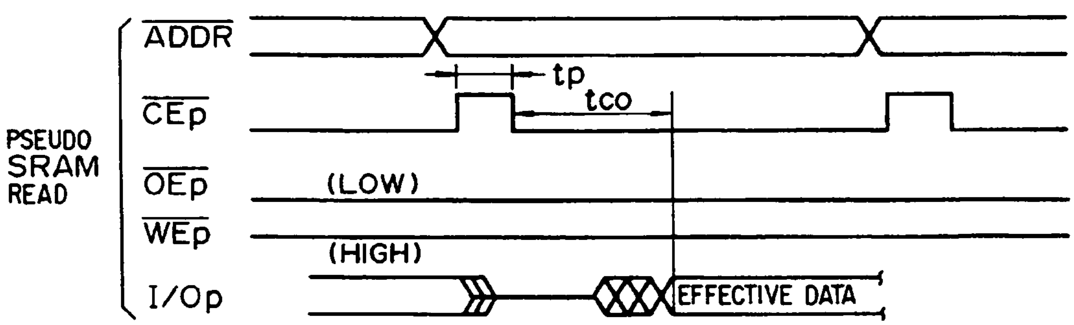
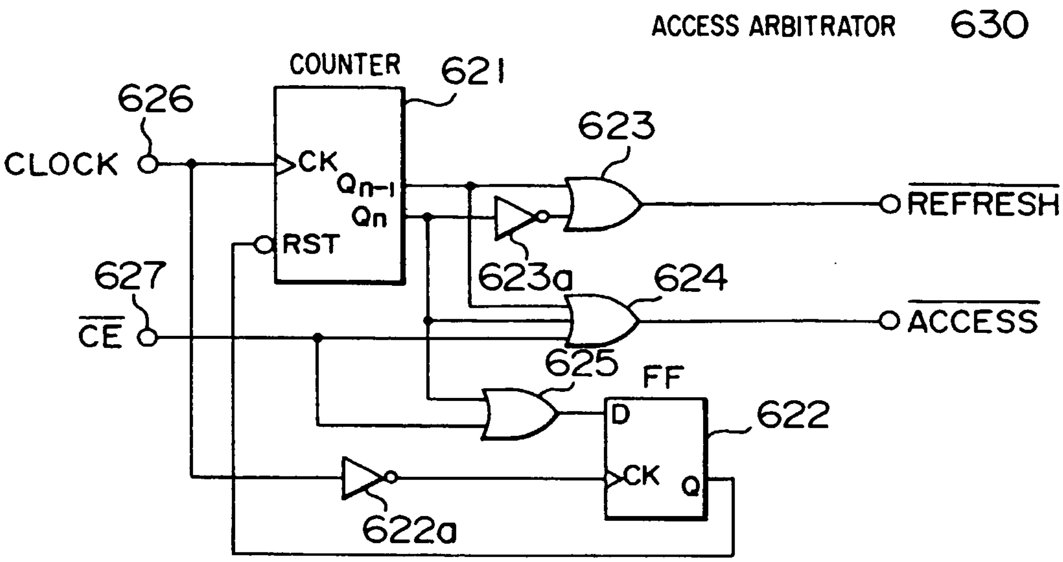

SRAM
READ
ADDR
CE
(LOW)
OE
(LOW)

FIG. 5B


PSEUDO
SRAM
READ
ADDR
tp
tco
CEp
OEp
(LOW)
WEp
(HIGH)
I/Op
EFFECTIVE DATA

EP 0 425 693 B1

F I G. 6

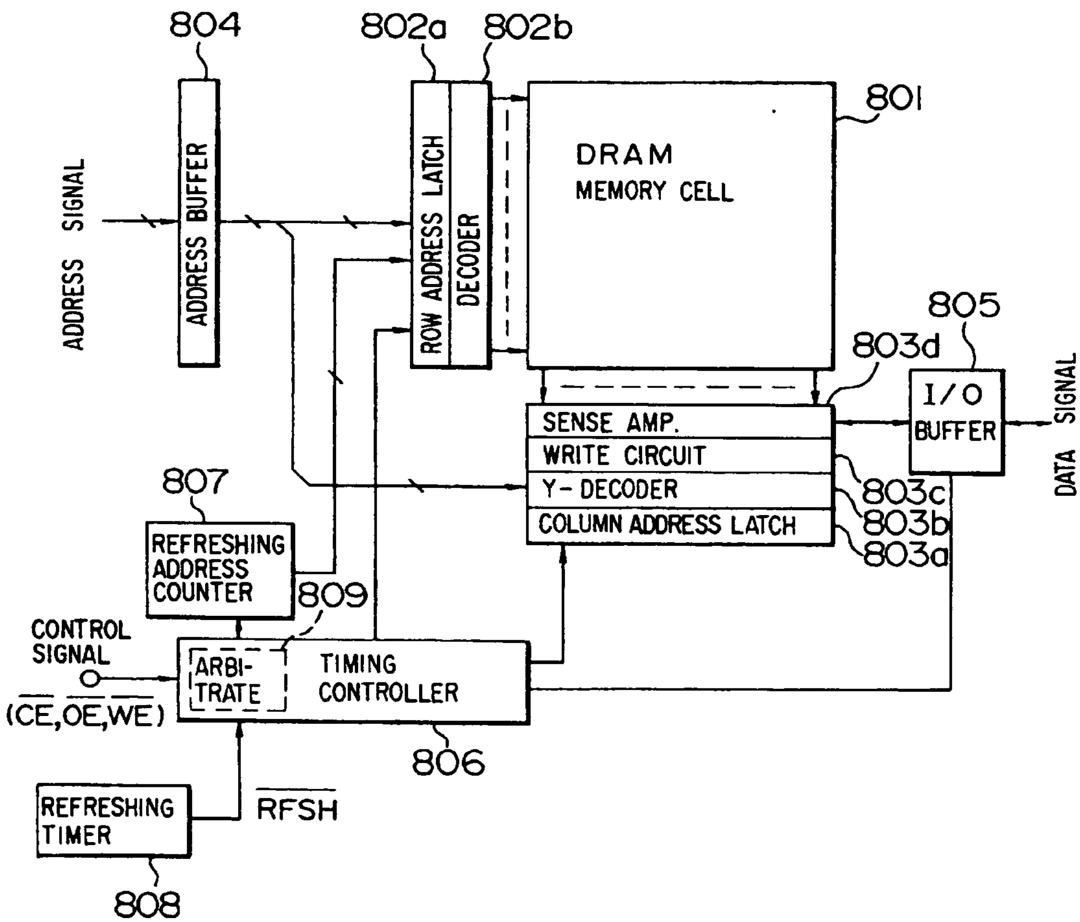


F I G. 7

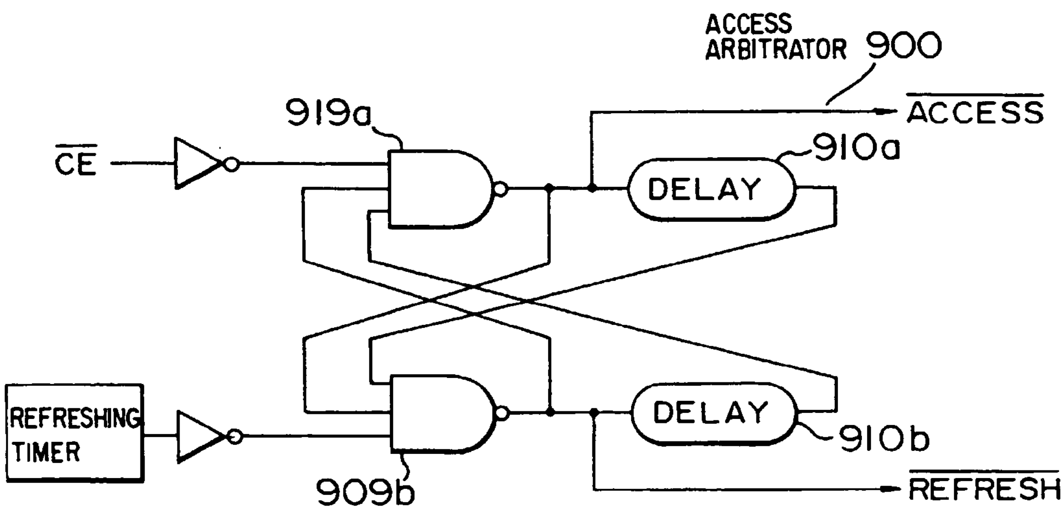
COUNTER OUTPUT

Q_{n-1}	Q_n	DURATION ALLOCATION
0	0	ACCESS ENABLE DURATION
1	0	PRECHARGE DURATION TO ACCESS
0	1	REFRESHING ENABLE DURATION
1	1	PRECHARGE DURATION TO REFRESHING
0	0	ACCESS ENABLE DURATION

F I G. 8

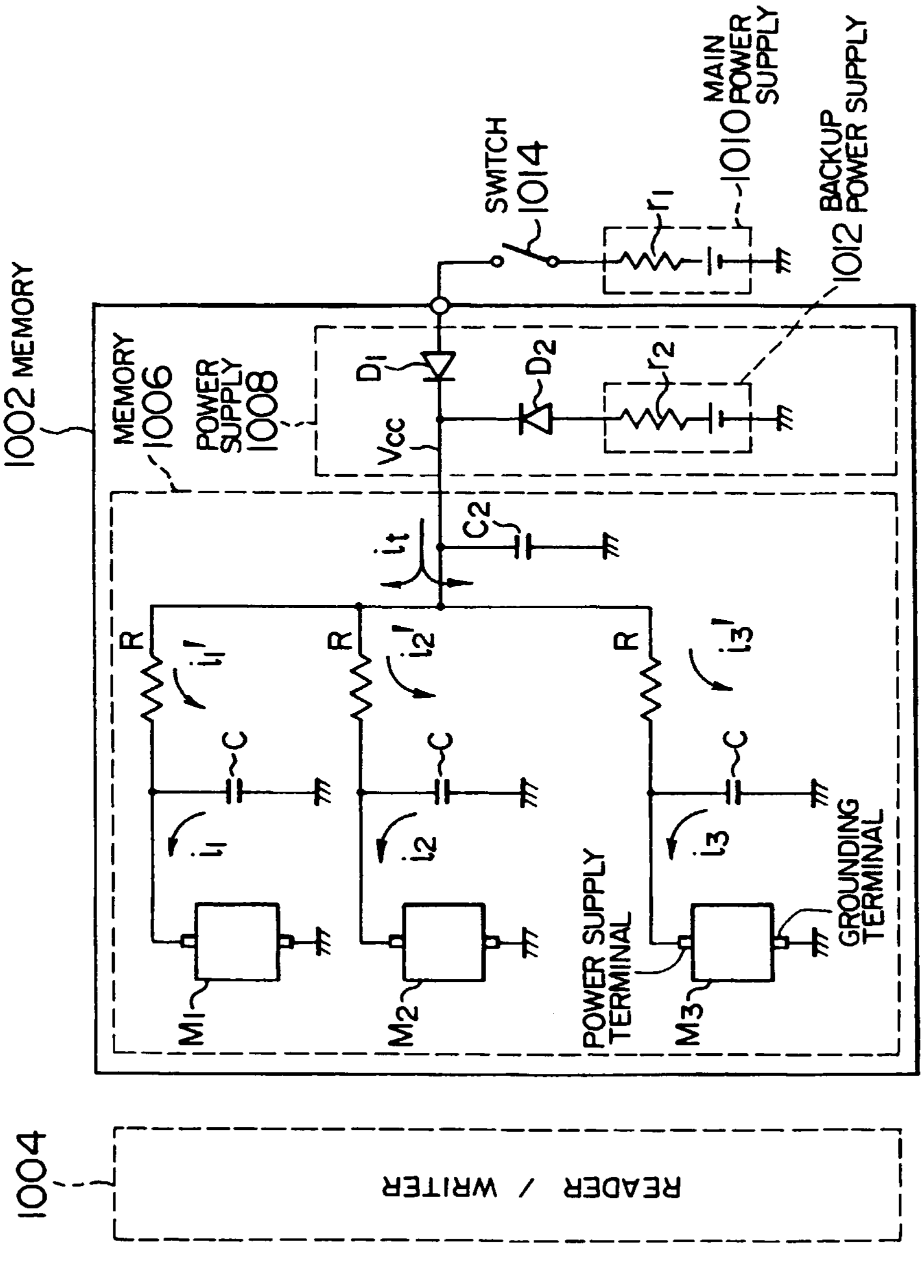

804
802a
802b
801
ADDRESS SIGNAL
ADDRESS BUFFER
ROW ADDRESS LATCH
DECODER
DRAM
MEMORY CELL
805
803d
I/O
BUFFER
DATA SIGNAL
SENSE AMP.
WRITE CIRCUIT
Y- DECODER
COLUMN ADDRESS LATCH
803c
803b
803a
807
REFRESHING ADDRESS COUNTER
809
CONTROL SIGNAL
(CE,OE,WE)
ARBI-TRATE
TIMING CONTROLLER
806
REFRESHING TIMER
RFSH
808

F I G. 9

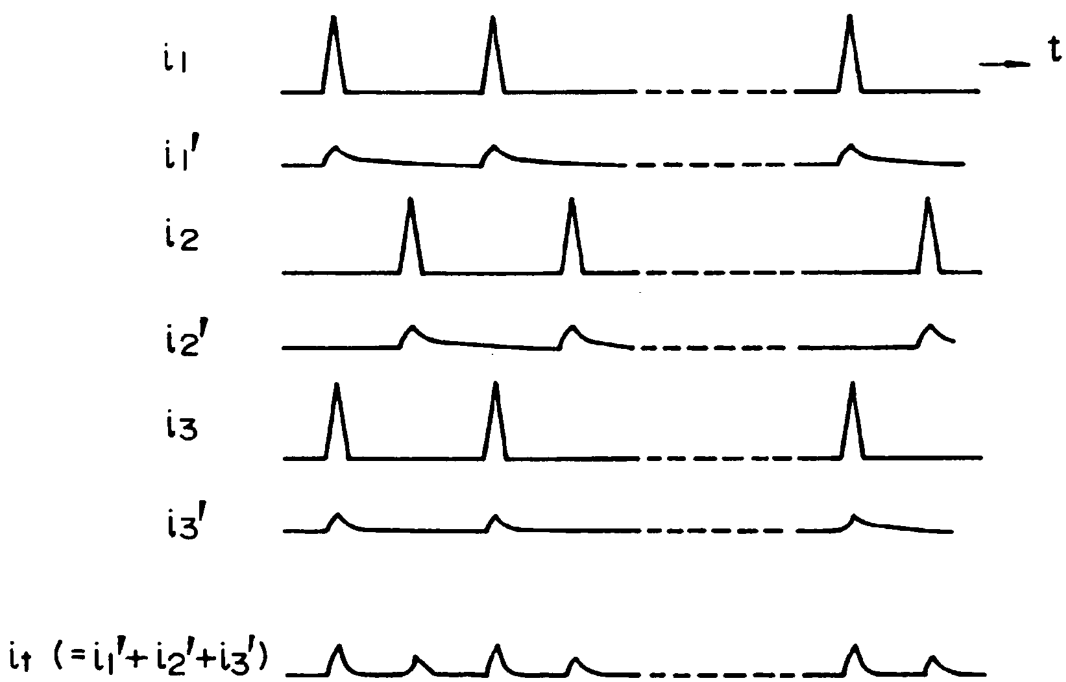

ACCESS ARBITRATOR 900
919a
$\overline{\text{CE}}$
DELAY
910a
$\overline{\text{ACCESS}}$
REFRESHING TIMER
DELAY
910b
909b
$\overline{\text{REFRESH}}$

EP 0 425 693 B1

F I G. 10A

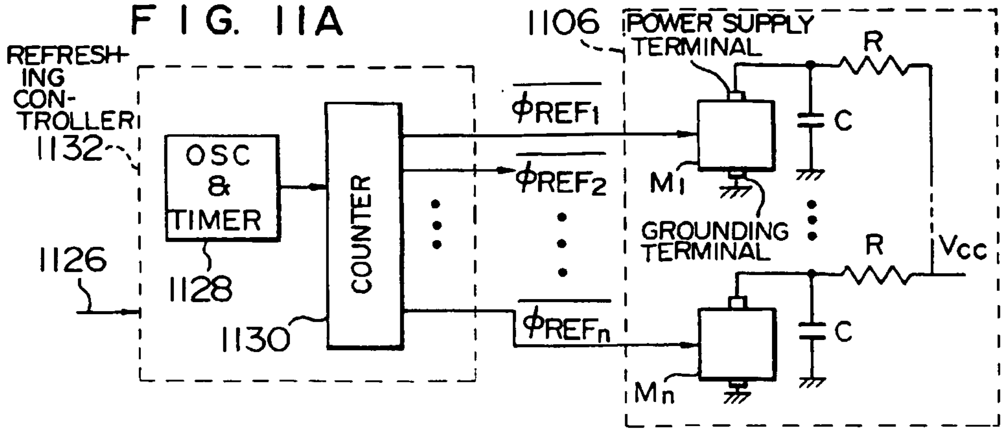


F I G. 10B

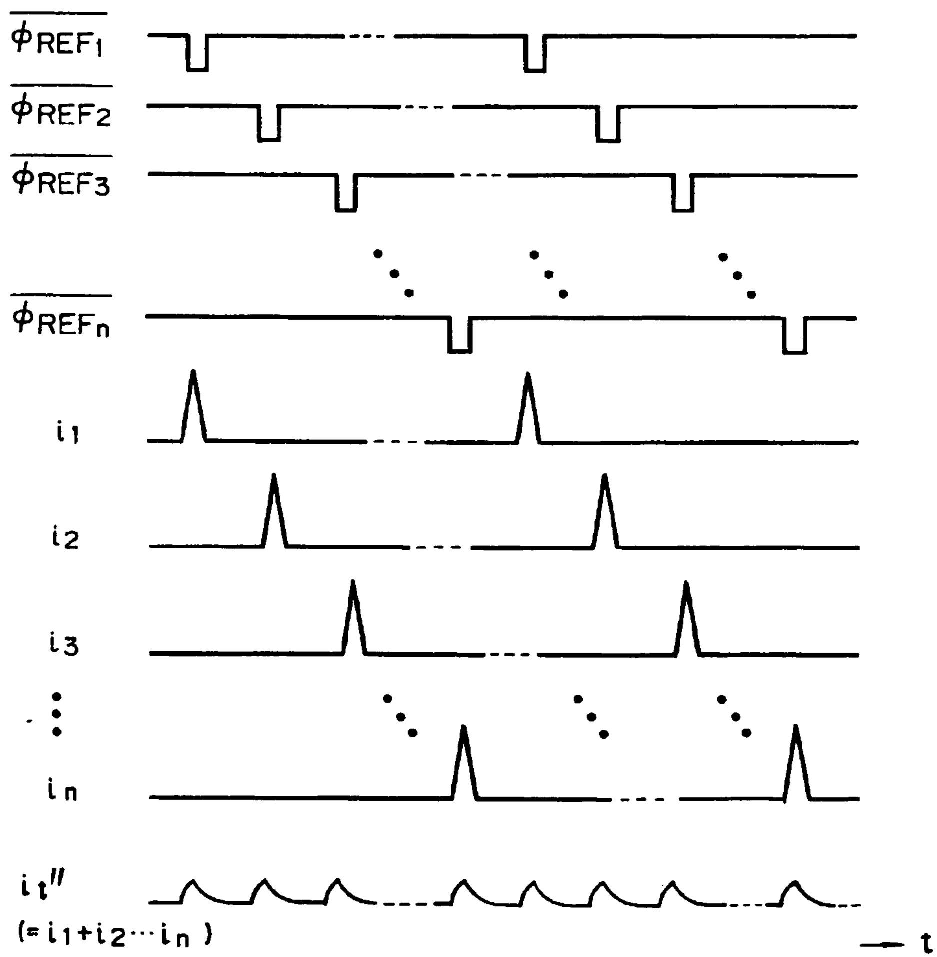


EP 0 425 693 B1

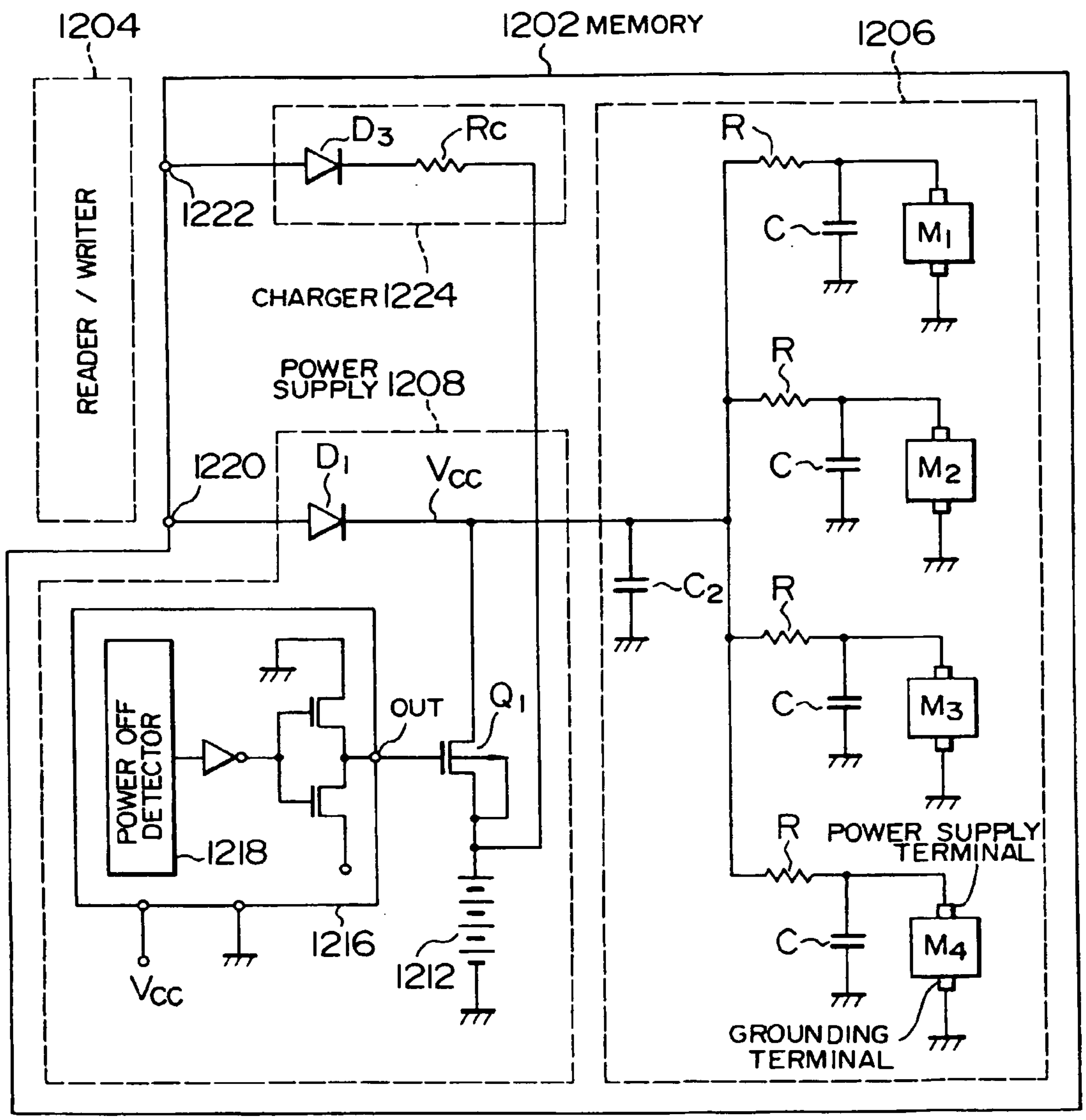
F I G. 11A



F I G. 11B

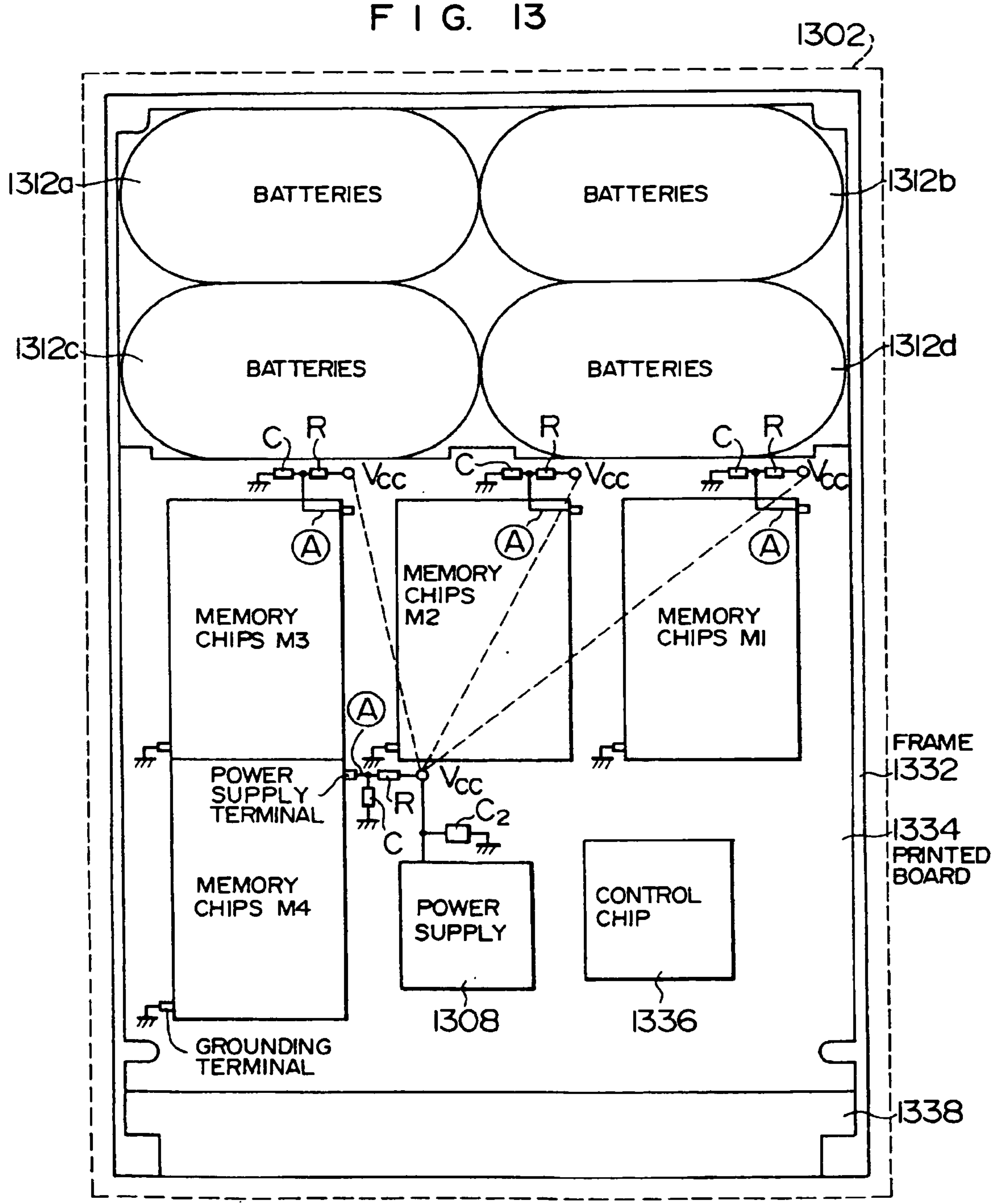


F I G. 12

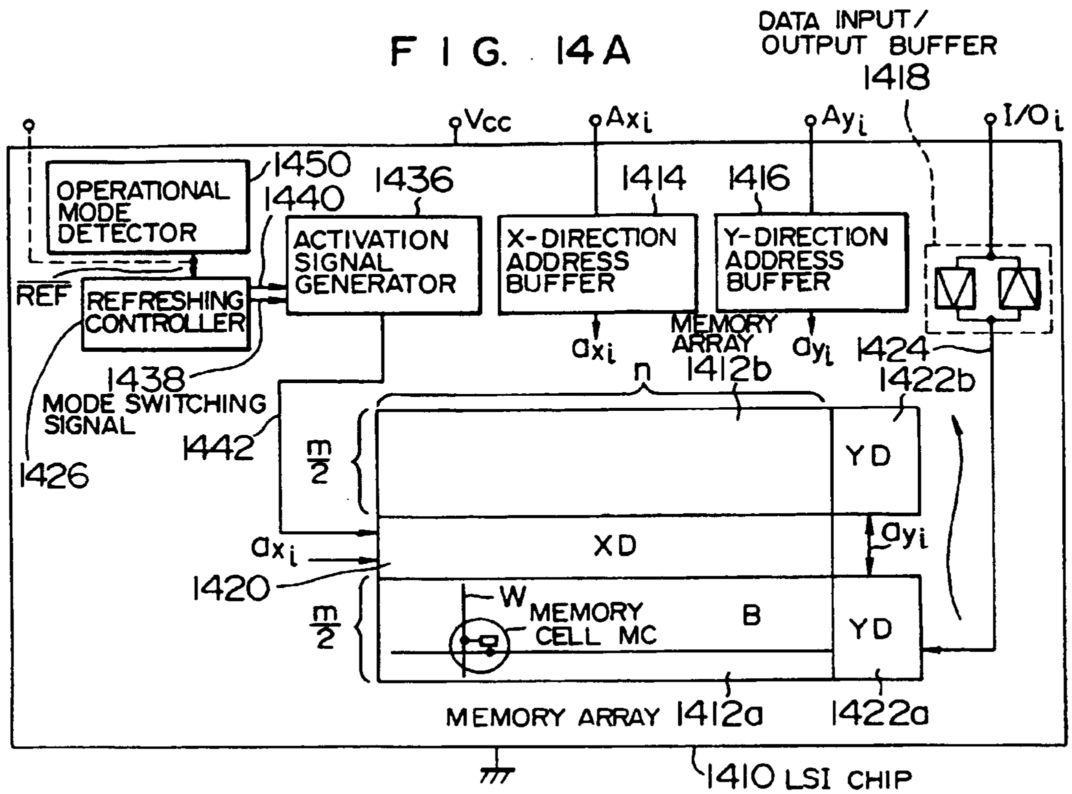

1204
1202 MEMORY
1206
READER / WRITER
D3
Rc
1222
CHARGER 1224
R
C
M1
POWER SUPPLY 1208
1220
D1
Vcc
M2
C2
M3
POWER OFF DETECTOR
1218
OUT
Q1
1216
1212
Vcc
POWER SUPPLY TERMINAL
M4
GROUNDING TERMINAL

EP 0 425 693 B1

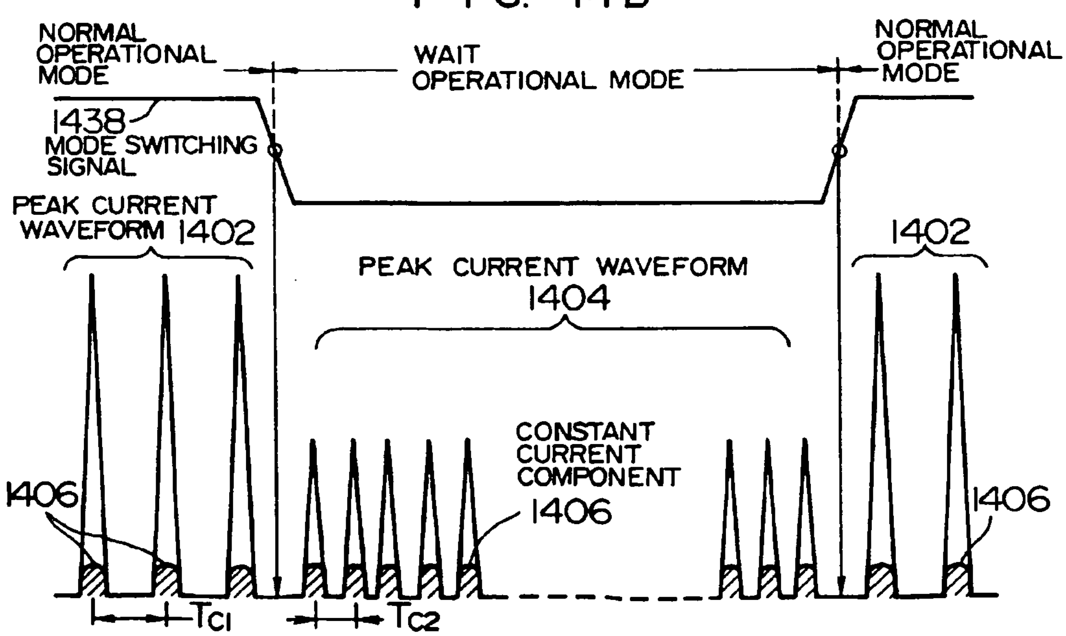
F I G. 13



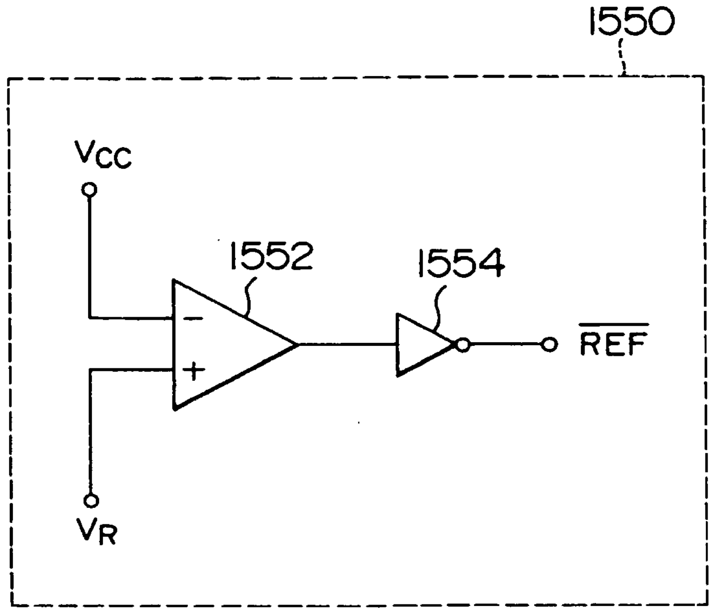
F I G. 14A



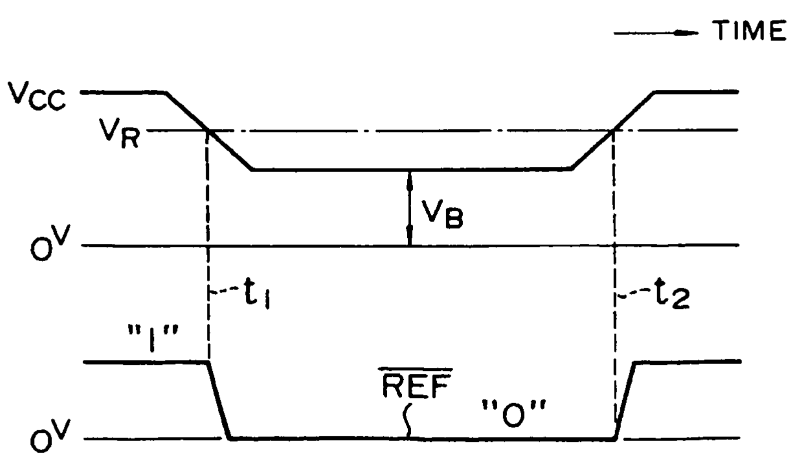
F I G. 14B



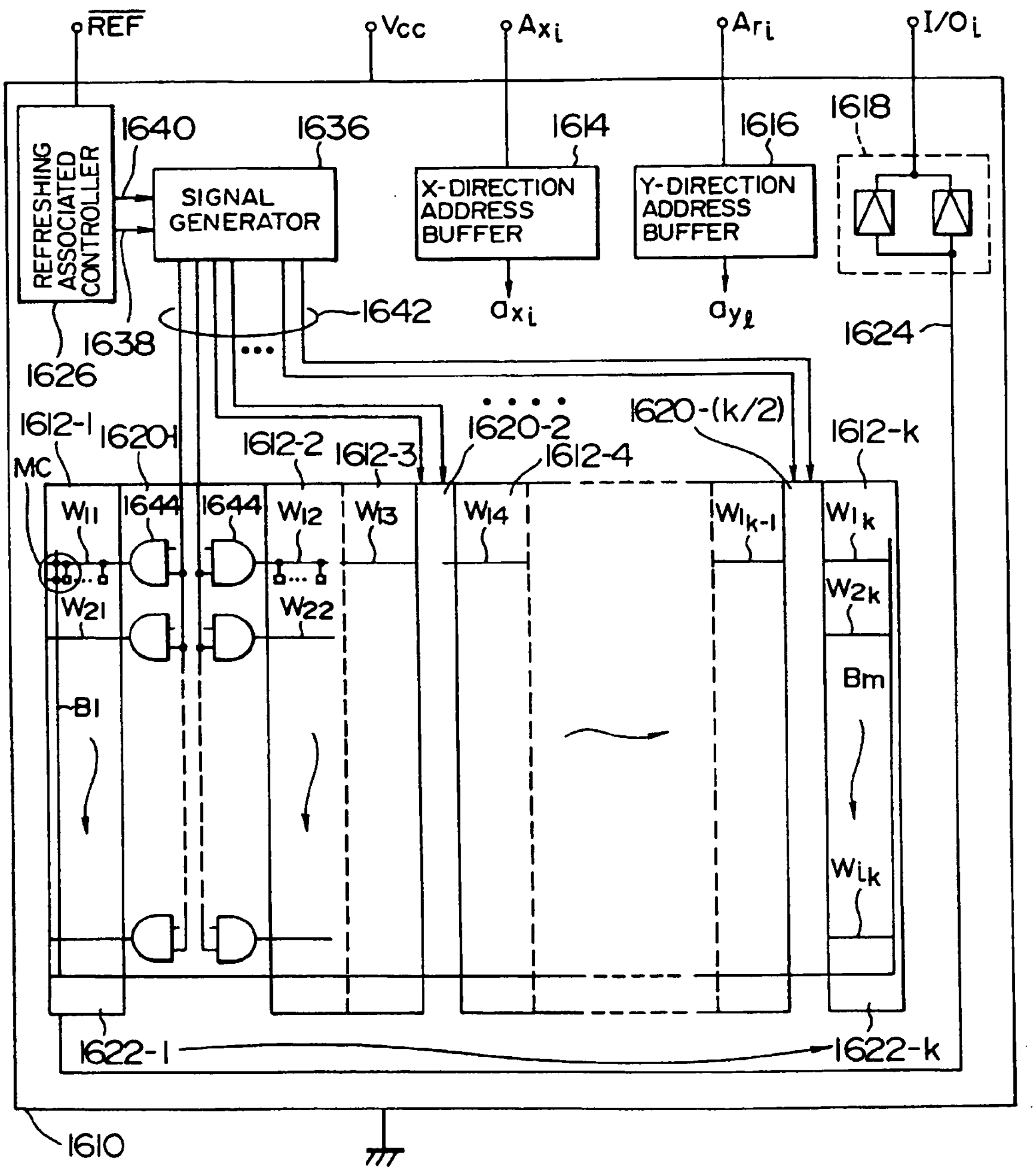
F I G. 15A



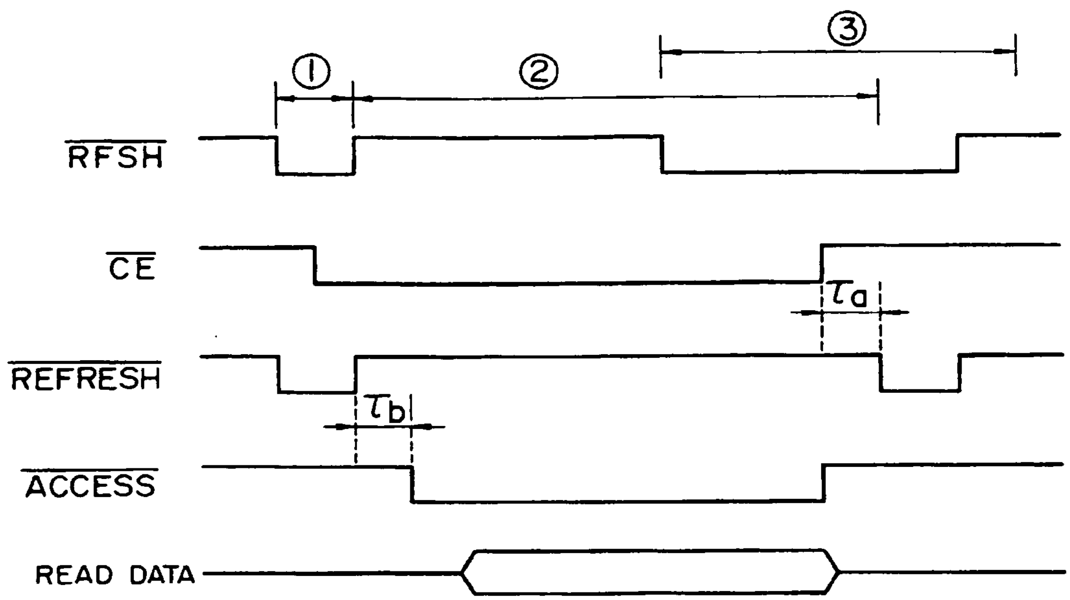
F I G. 15B



F I G. 16

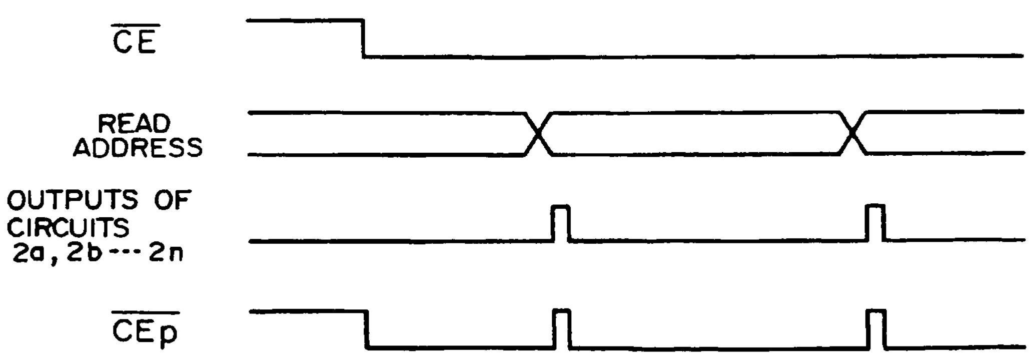

REF
Vcc
Ax_i
Ar_i
I/O_i
REFRESHING ASSOCIATED CONTROLLER
1640
1636
SIGNAL GENERATOR
1614
X-DIRECTION ADDRESS BUFFER
1616
Y-DIRECTION ADDRESS BUFFER
1618
1642
ax_i
ay_ℓ
1638
1626
1624
1612-1
1620-1
1612-2
1612-3
1620-2
1612-4
1620-(k/2)
1612-k
MC
W11
1644
1644
W12
W13
W14
W1k-1
W1k
W21
W22
W2k
B1
Bm
Wik
1622-1
1622-k
1610

F I G. 17



①
②
③
RFSH
CE
τa
REFRESH
τb
ACCESS
READ DATA

F I G. 18



CE
READ ADDRESS
OUTPUTS OF CIRCUITS 2a, 2b --- 2n
CEp

EP 0 425 693 B1

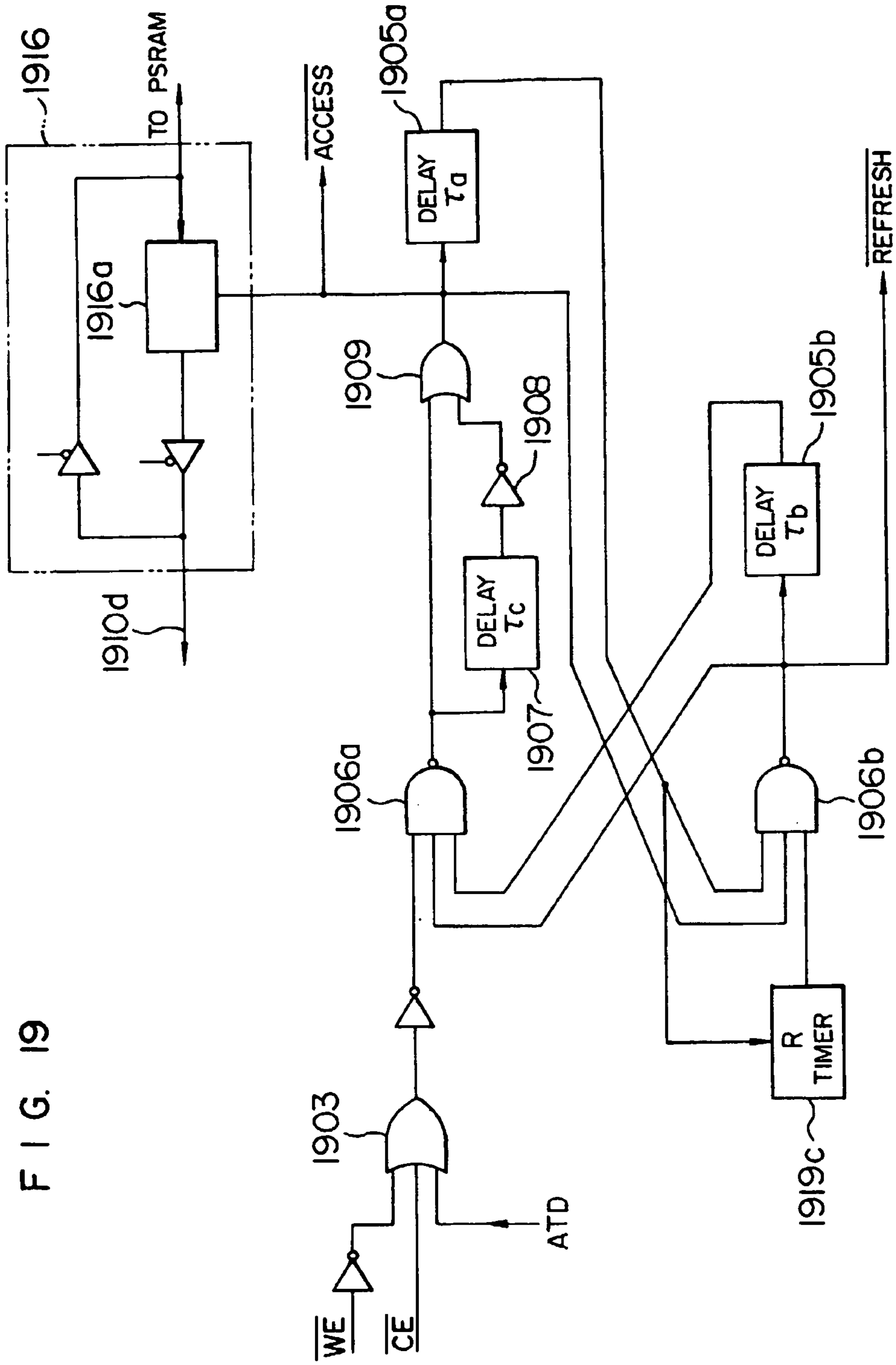
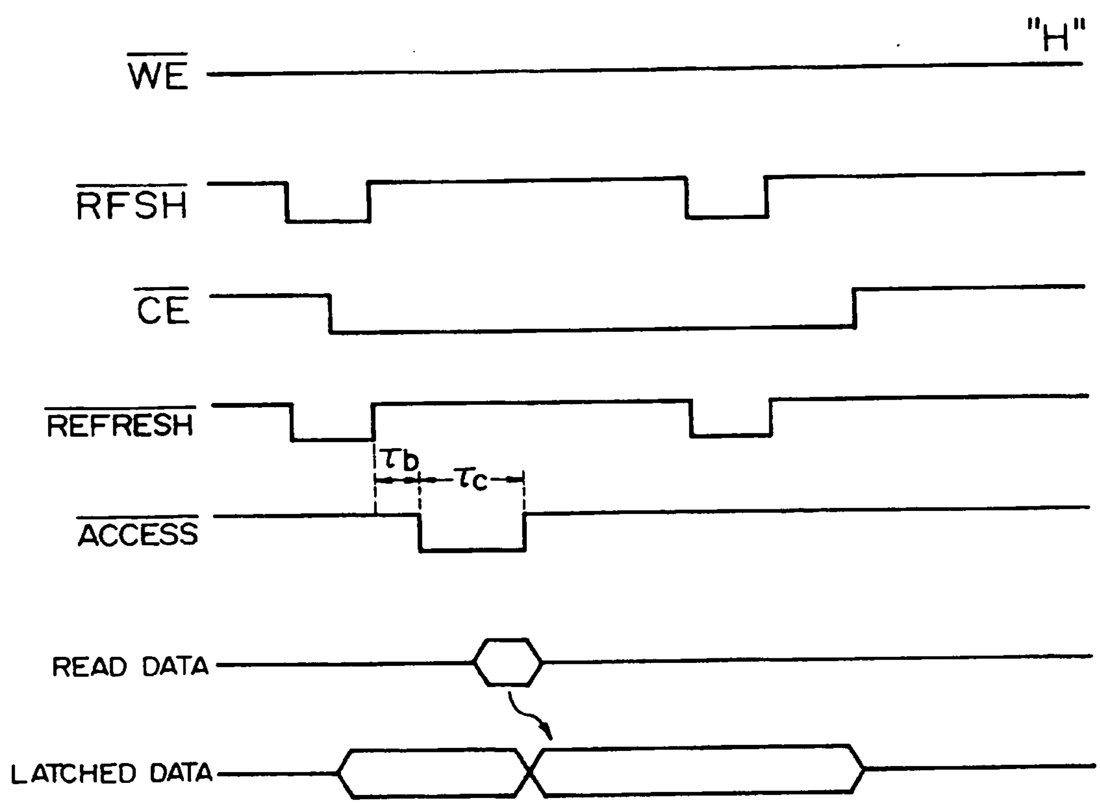


FIG. 19

FIG. 20


"H"
$\overline{WE}$
$\overline{RFSH}$
$\overline{CE}$
$\overline{REFRESH}$
τb
τc
$\overline{ACCESS}$
READ DATA
LATCHED DATA

EP 0 425 693 B1

F I G. 21

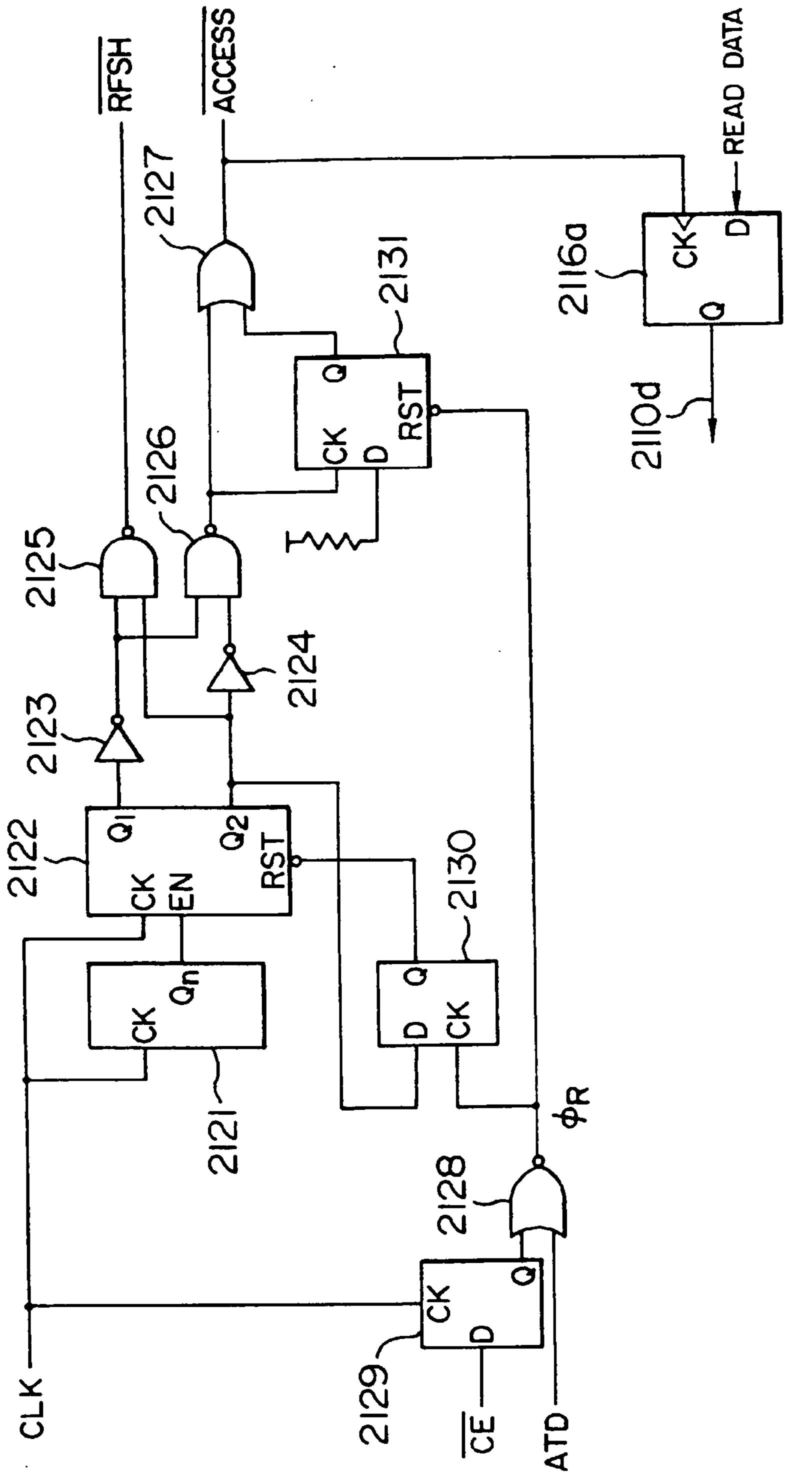


FIG. 22A

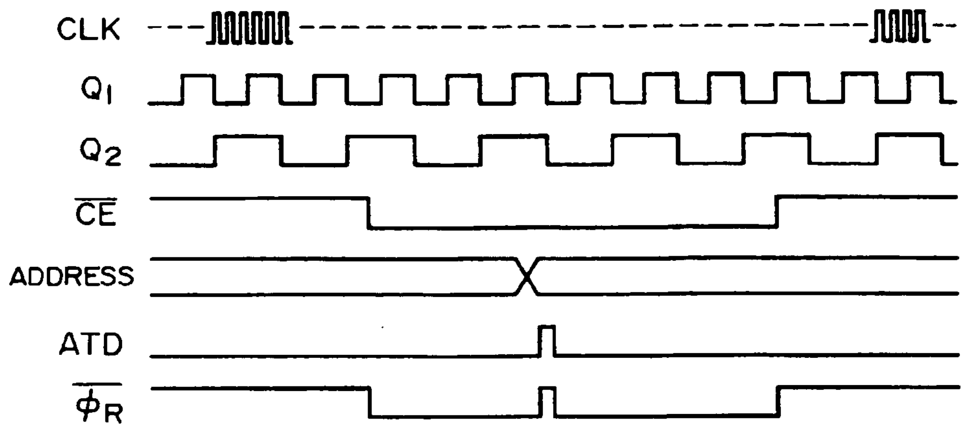


FIG. 22B

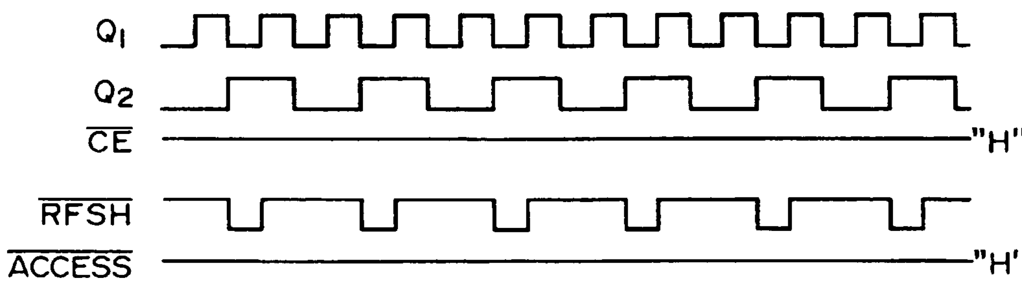


FIG. 22C